Design and Verification for 3G Wireless RFICs

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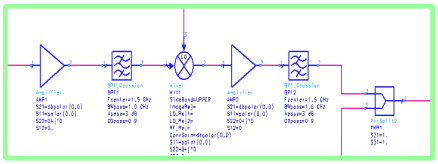
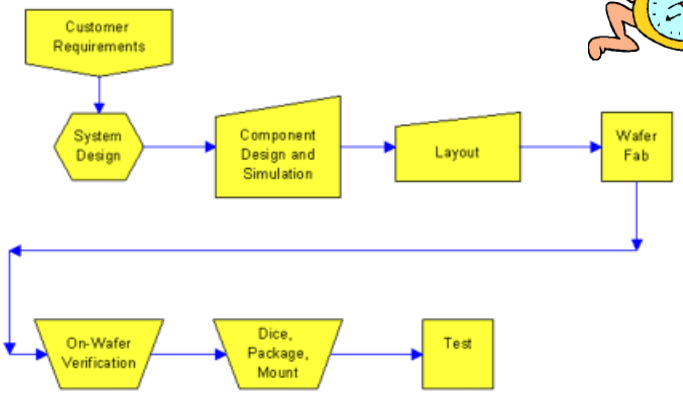
Innovating the HP Way

Requirements for the Power Amplifier of 3G Wireless Handsets

- Balance conflicting requirements
  - Efficient battery usage
  - Distortion in all its forms
- Include several alternative designs to choose best
- Satisfy specifications of communication format
- Minimize time to market



Typical Development Design Flow



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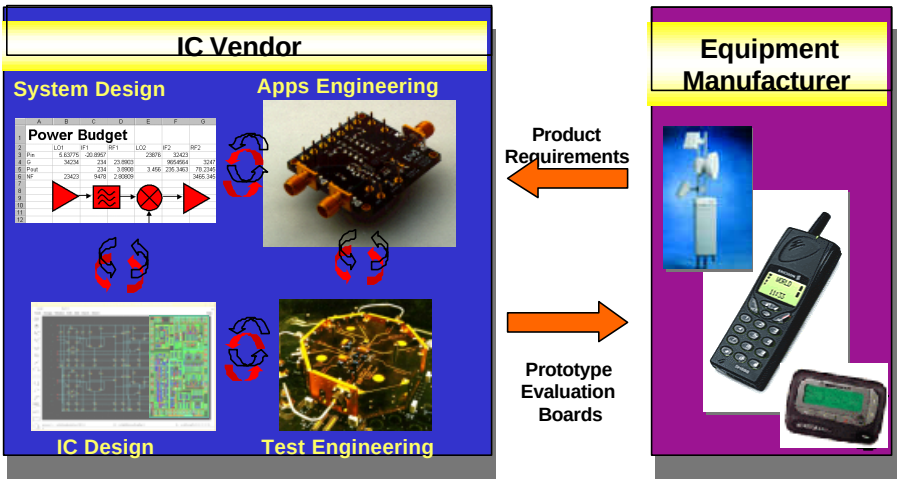
IC Vendor to Customer Linkages



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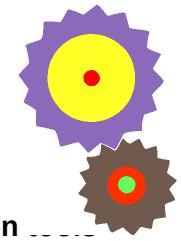
Design Challenges for 3G Wireless Handset Power Amplifiers – Synergism of Design and Test System Required

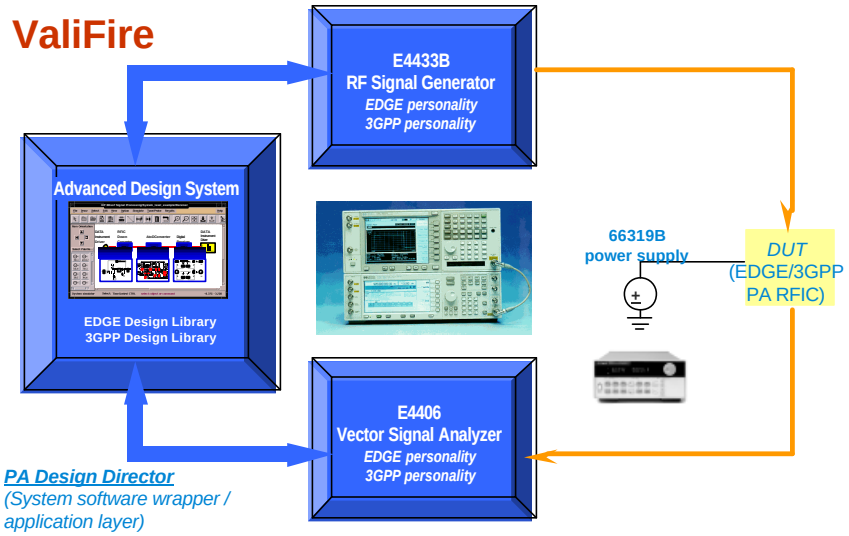


- Minimize the need for wafer design turn-arounds
  - Include alternative designs on wafer
  - Use accurate (validated) models with simulation
- Account for module parasitics
- Account for application board components
- Test the design with virtual test equipment
- Speed up and automate actual testing

The Many Tasks of Testing

- Assemble test equipment
- Develop procedures
- Assure procedures satisfy the latest format specifications
- Perform tests
  - Test the different designs on the wafer
  - Vary bias
  - Vary temperature
  - Test a statistically valid sample
- (This takes weeks and uses critical resources – especially people.)

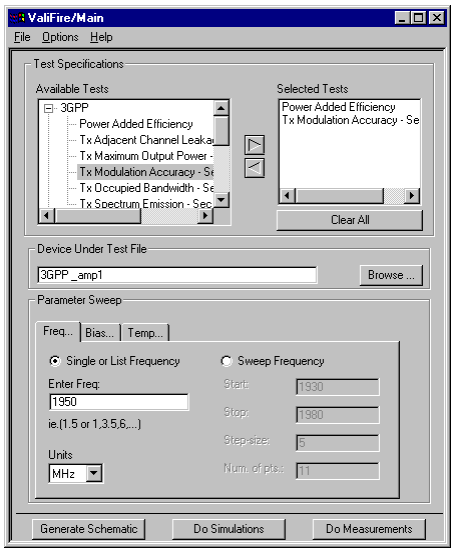
Agilent's Handset PA ValiFire System



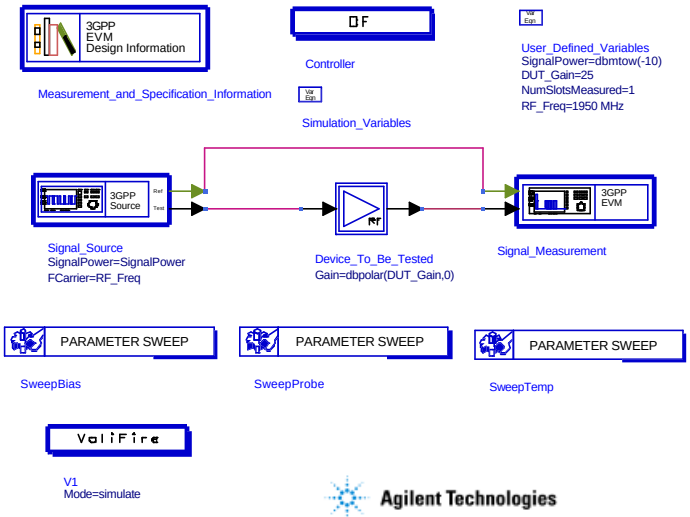
Test Automation

Sequence and automate your prototype tests

- **Built-in 3G test specs**
- **Guided user interface**
- **Data collection**
- **Spec checking**

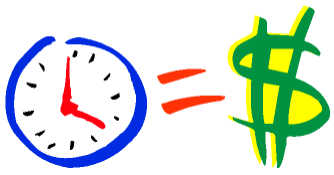


ADS Switches Between Simulation (Virtual) & Measurement (Actual)

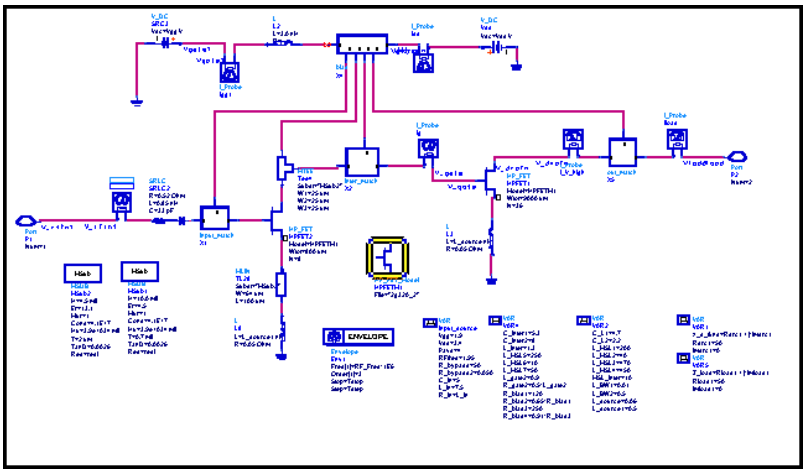


Common Bottlenecks During Design

- Waiting for completed chips from the wafer
- Simulating and evaluating the package's effect
- Design of the application board and simulating and evaluating its effect
- Testing (each specification at varying bias & temperature)
- Correlation of test results with customer needs & results



A Design of a Power Amplifier Chip



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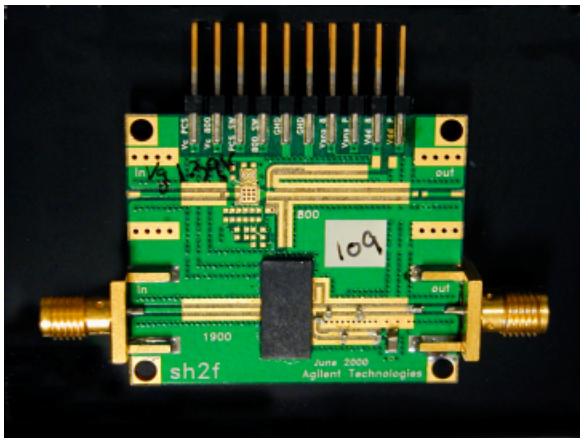
Verification of Module/Package Application Board



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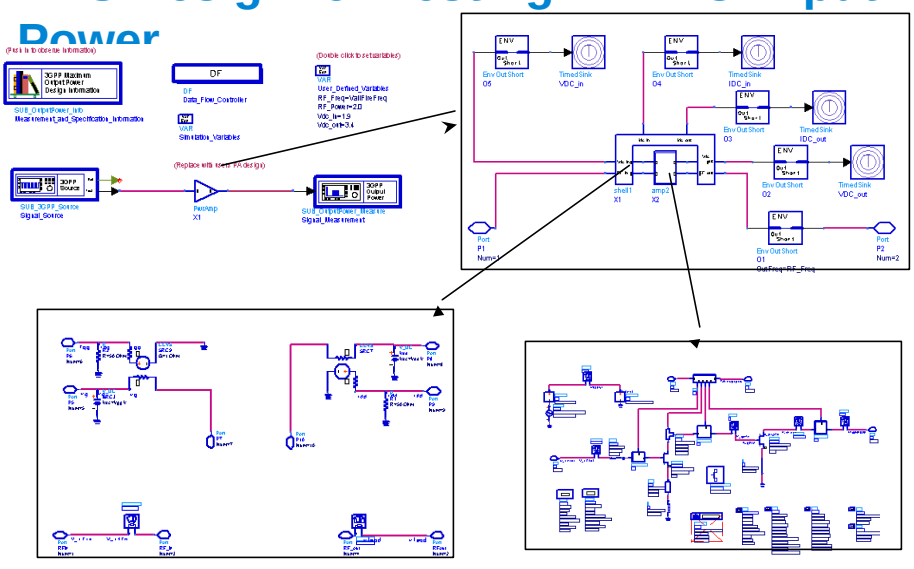
Critical Tests for 3G Handset Power Amplifier Design

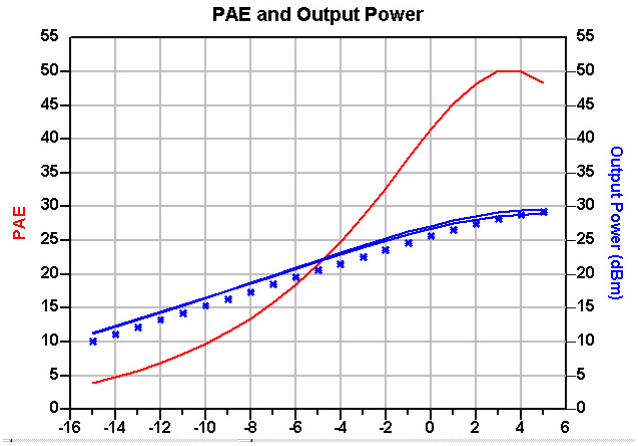
- **Both Virtual & Actual**
- **Power added efficiency (PAE)**
- **Power vs. frequency**
- **Error Vector Magnitude (EVM)**
- **Adjacent channel leakage ratio (ACLR)**

- **Actual Verification**
- **Controlled by ADS with ValiFire**
  - **Operates test equipment**
  - **Includes test specs**
    - **Quick updates**
  - **Varies bias**
  - **Can control ovens**
  - **Collects data**

ADS Design for Testing PAE vs. Input Power



Data Showing PAE vs. Input Power



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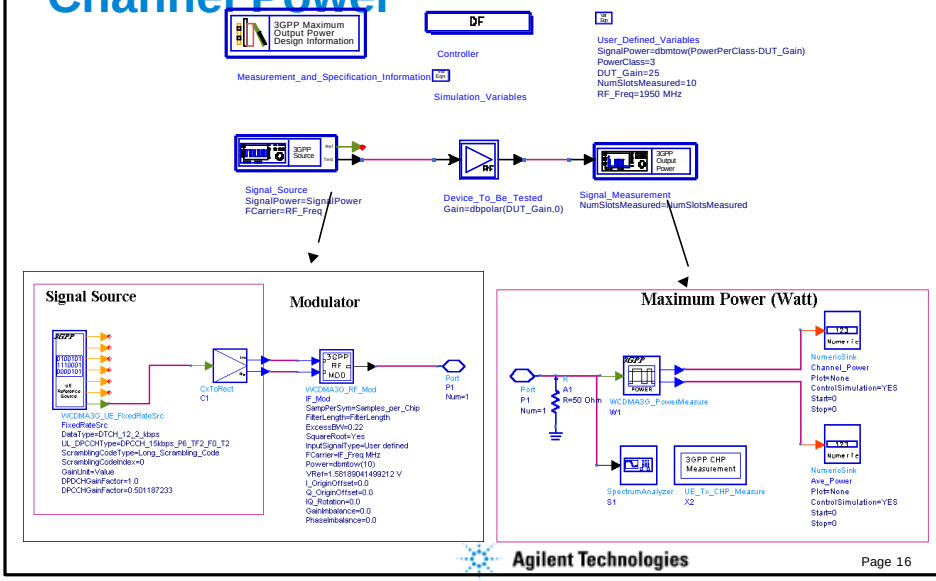
ADS Design for Testing Complex Channel Power



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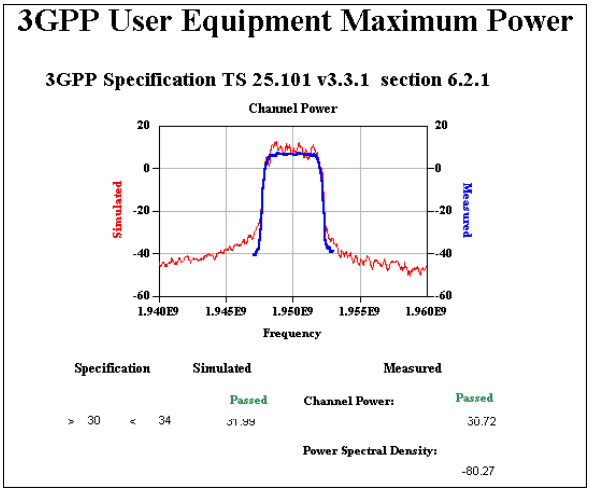
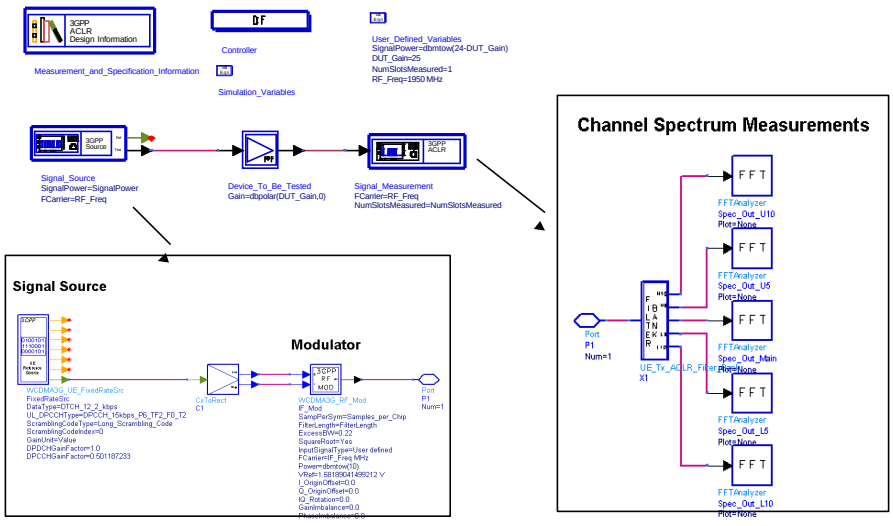
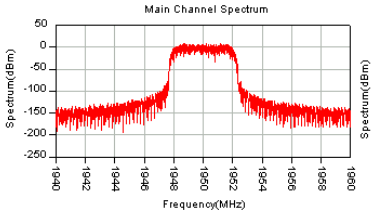
Data Showing Complex Channel Power

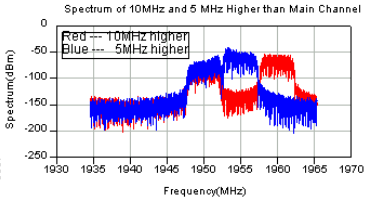


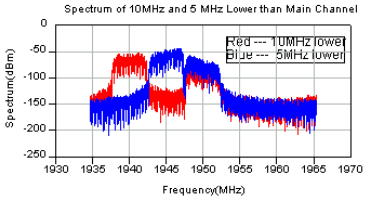
ADS Design for Testing ACLR



Data Showing ACLR







ACLR (dB)

ACLR_U10	ACLR_U5	ACLR_L5	ACLR_L
63.817034	54.726446	55.060329	63.690

UE ACLR

Power Class	UE Channel	ACLR limit
3	+5 MHz or -5 MHz	33 dB or -50 dBm whi
3	+10 MHz or -10 MHz	43 dB or -50 dBm whi
4	+5 MHz or -5 MHz	33 dB or -50 dBm whi
4	+10 MHz or -10MHz	43dB or -50 dBm whic

Simulated vs. Measured ACLR

3GPP ValiFire Adjacent Channel Leakage power Ratio (ACLR)

3GPP Specification TS 25.101 V3.2 section 6.6.2.2

Simulated PASSED

Main Channel Pwr	26.47			
	Lower		Upper	
Offset Frequency	dBc	dBm	dBc	dBm
5.00 MHz	-38.14	-11.67	-38.72	-12.255
10.00 MHz	-53.57	-27.10	-53.76	-27.290

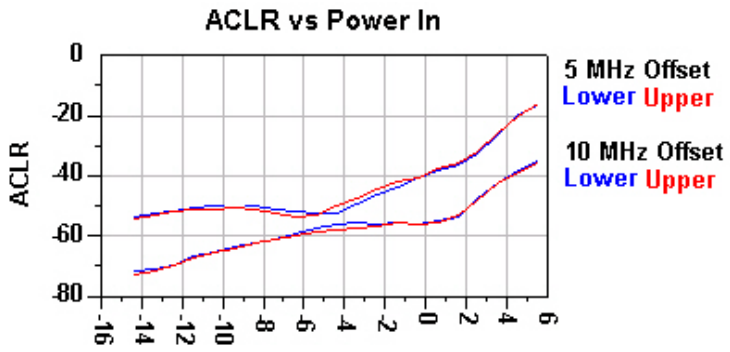
Measured PASSED

Main Channel Pwr	27.39			
	Lower		Upper	
Offset Frequency	dBc	dBm	dBc	dBm
5.00 MHz	-40.07	-12.68	-39.13	-11.746
10.00 MHz	-55.72	-28.34	-55.99	-28.599

Specification requirements

+5 MHz or -5 MHz	33 dB or -50 dBm which ever is higher
+10 MHz or -10 MHz	43 dB or -50 dBm which ever is higher

Measured ACLR vs Input Power



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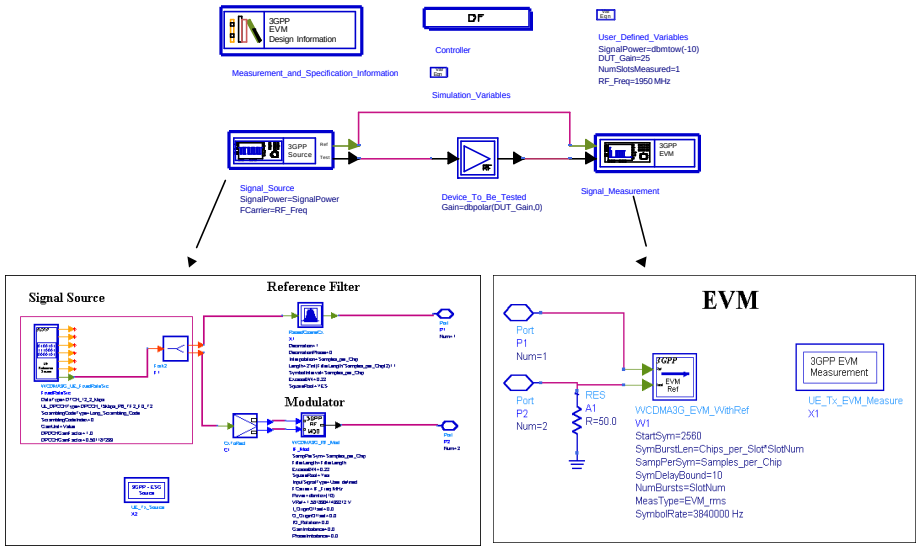
ADS Design for Testing EVM



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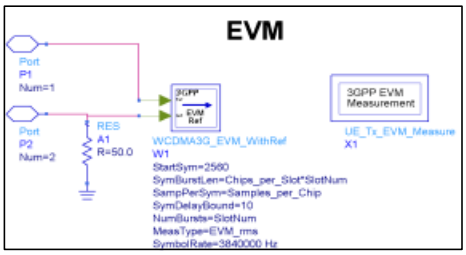
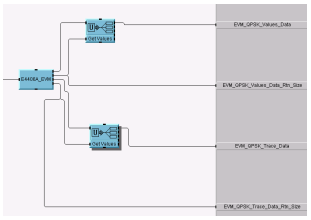
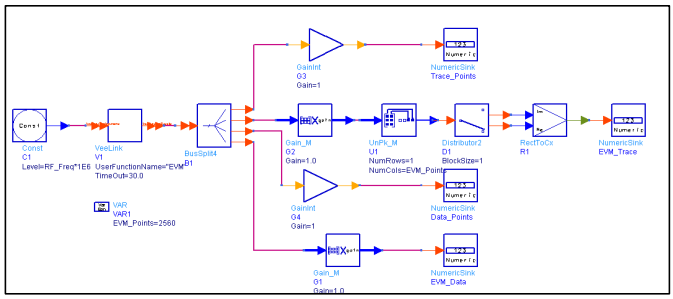
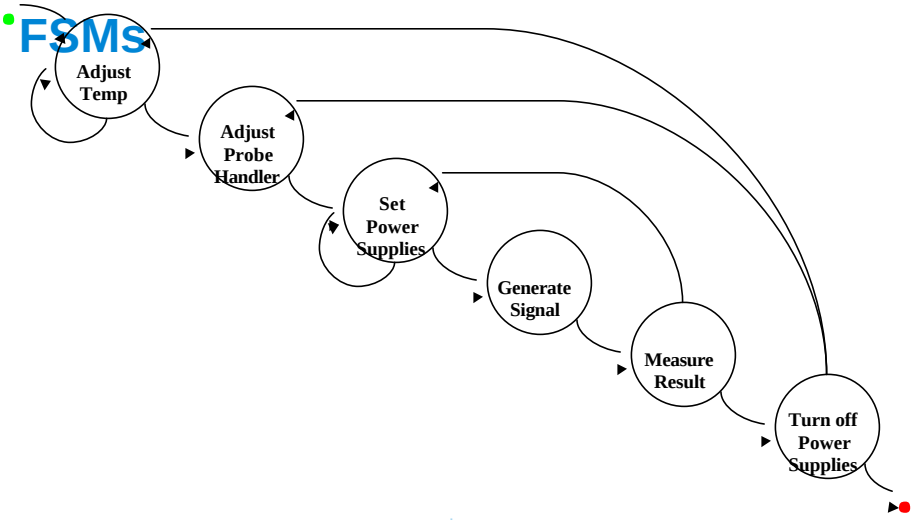
Instruments Link to ADS via VEE



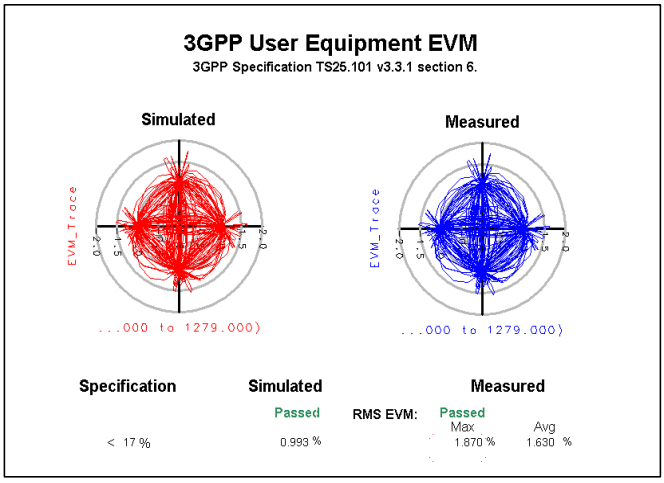




Measurement system can be modeled as mix of Dataflow and FSMs



Data Showing EVM



Data showing EVM

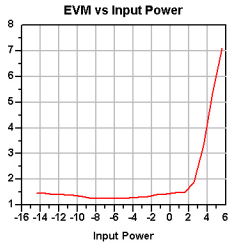
3GPP ValiFire Error Vector Magnitude (EVM)

3GPP Specification TS 25.101 V3.2 section 6.8.2

Simulated (%)	Measured (%)
5.061	1.430E-10
PASSED	PASSED

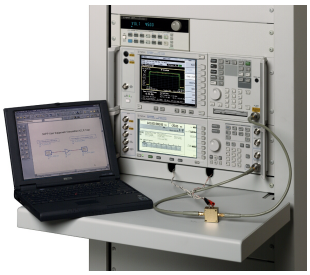
Specification requirements

The modulation accuracy EVM shall not excess 17.5% at the maximum output power



There's a Lot of Data. We Still Need to Vary Bias and Test Many Devices. Then What About Spec Changes?

- That's a LOT of documented data to be taken and processed
  - ValiFire automates:
    - Instrument operation
    - Data collection
    - Specification checking
  - Agilent updates procedures for format spec changes

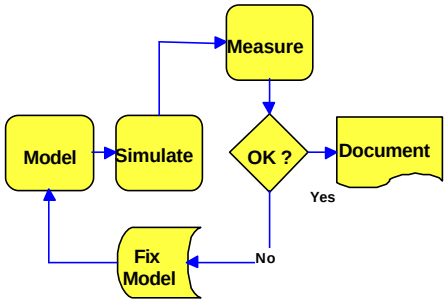


These Techniques Provide the Mechanism to Correlate RFIC Supplier and NEM Results and Requirements

- The NEMs cannot afford to be tied to a sole source supplier.
- They need to validate alternative suppliers to use when a specific supplier

Reconcile Differences Between Virtual and Actual Performance for Better Future Designs

- This is the way to achieve accurate design models
  - It helps reduce the number of design cycles



Conclusion: Significant Time and Trouble Saved with Synergistic Chip Design and Integrated Test

- Module and application board parasitics included.
- Virtual test for correlation of design with actual test results and accurate modeling.
- Test procedure updates readily available as specs mature.
- Test procedures and specification checking are automatic.
- Statistically valid sample size needed.