Integrating the JHDL Design Environment into Ptolemy-II

Michael J. Wirthlin
wirthlin@ee.byu.edu
Brigham Young University
Provo, UT 84602

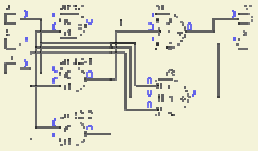
Ptolemy Miniconference
Berkeley, CA, March 22-23, 2001

JHDL Background

- **JHDL is a structural hardware design tool based on Java**
  - Circuits are described by creating Java classes
    - Users instance circuit objects (primitives/composite)
    - Circuits wired together with Wire objects
  - JHDL supports several FPGA design libraries
- **Supports low-level design specification for creating optimized module generators**
  - Logic mapping
  - Circuit placement
- **http://www.jhdl.org**

JHDL Example*

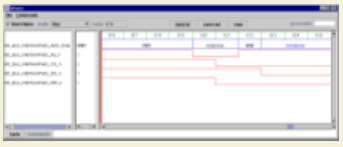
```
public class FullAdder extends Logic {

/* Define the ports for a 1-bit full adder */

  public static CellInterface cell_interface[] = {
    in("a",1), in("b",1), in("ci",1),
    out("s",1), out("co",1)
  };

  public FullAdder(Node parent,Wire a, Wire b,
                   Wire ci,Wire s, Wire co) {
    super(parent);

    Wire t1 = new Xwire(this,1);
    Wire t2 = new Xwire(this,1);
    Wire t3 = new Xwire(this,1);
    new and2(this,a,b,t1);
    new and2(this,a,ci,t2);
    new and2(this,b,ci,t3);
    new or3(this,t1,t2,t3,co);/* co is carry out */
    new xor3(this,a,b,ci,s);  /* s is output */
}
```

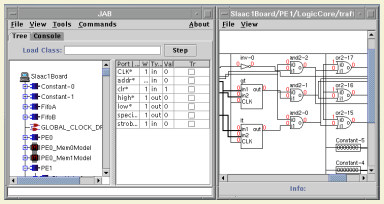


** Some necessary details have been removed for brevity*

JHDL Tools

- Waveform Viewer
- Schematic Viewer
- Module Generator Libraries
- Hierarchy Browser
- Circuit Simulator

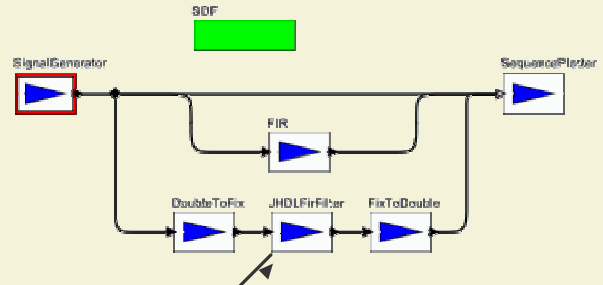




Motivation for Integrating JHDL/PT-II

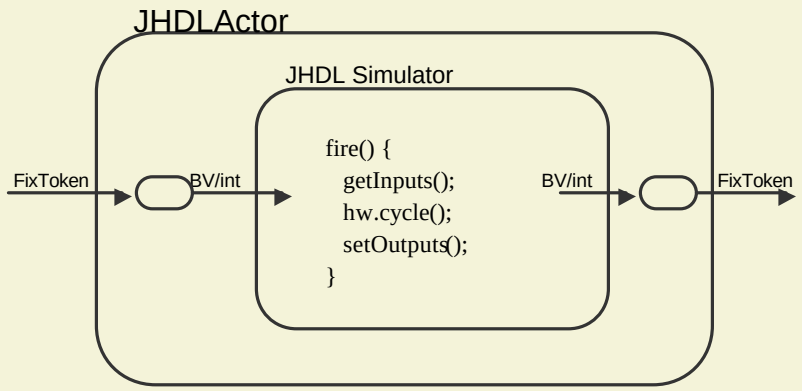
- Ptolemy provides excellent testbench capability for JHDL circuits
  - Mature, growing library (primarily interested in DSP)
  - Opportunity for multi-domain simulation (DE, PN, SDF, etc.)
  - Quickly prototype sophisticated testbenches
  - Exploit graphical results in Ptplot
- Support a design methodology of gradual refinement
  - Algorithmic exploration using Ptolemy actors
  - Architectural exploration using JHDL circuits
  - Mix JHDL circuits with high-level Ptolemy actors
- Test/Expand JHDL foreign interface functionality

System Example



JHDL Circuit
- Cycle accurate
- Bit-accurate
- Simulates using JHDL simulator
- Built using Xilinx FPGA primitives

JHDL Actors Within Ptolemy



Current Approach

- JHDL actors currently used only with SDF
- Managing Timing: fire vs. JHDL clocks
  - Convert data at input ports to JDHL circuit types
  - Execute specified number of JHDL clocks
  - Convert JHDL circuit ports to Ptolemy types
- Type Conversion
  - JHDL circuit inputs are all bits and bit_vectors
  - JHDL actor ports must use FixToken
  - FixToken tokens must be converted to JHDL BV/int

Demonstrations

- JHDL Actors
  - Multiplication (constant and non-constant)
  - Arithmetic operators
  - Logic operators
- JHDL FirFilter
  - Arbitrary tap FIR filter
  - Arbitrary multiplier precision
  - Uses opto
- FPGA Download Actor
  - Design operating on actual FPGA resources
  - Interface to FPGA board through JHDLActor

Future Work

- Improved manipulation of FixPoint precision
- Additional JHDL actors
- Support other domains
- Improve efficiency of JHDL interface
- Integrate FSM domain and support circuit FSMs