Ptolemy II in Embedded Signal Processing Architectures: Deriving Process Networks From Matlab

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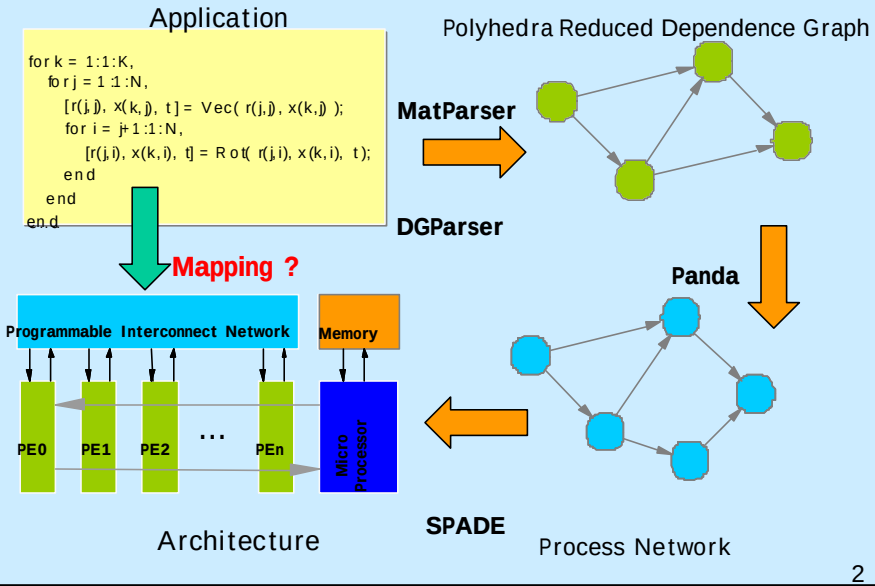
Problem



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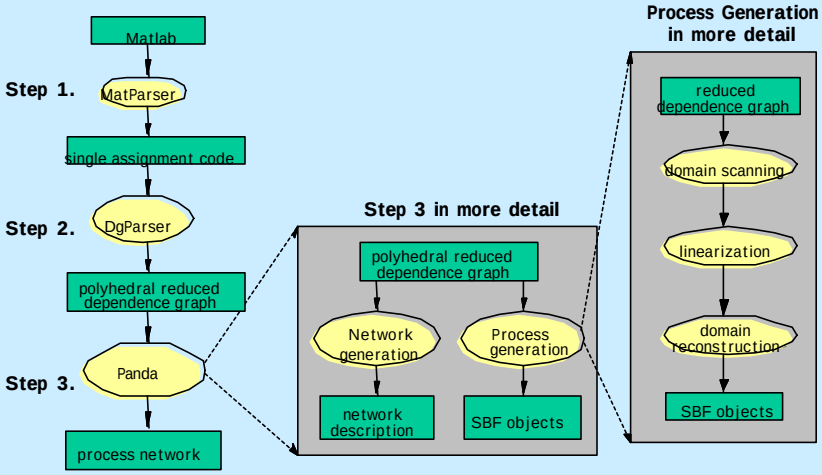
Compaan



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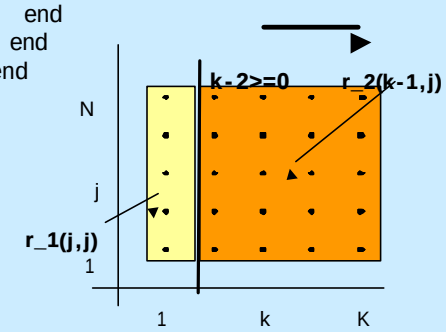
Step 1: MatParser

Array Dataflow Analysis

```
for k=1:1:K,
  for j=1:1:N,
    [r(j,j),x(k,j),t]=Vec(r(j,j),x(k,j));
    for i=j+1:1:N,
      [r(j,i),x(k,i),t]=Rot(r(j,i),x(k,i),t));
    end
  end
end
```




```
for k = 1 : 1 : K,
  for j = 1 : 1 : N,

    if k-2>= 0,
      [ in_0 ] = ipd( r_2( k-1, j ) );
    else %% if -k+1 >= 0
      [ in_0 ] = ipd( r_1( j, j ) );
    end

  [ out_0,out_1,out_2 ] = Vec( in_0, in_1 );

    [ r_1( k, j) ]  = opd( out_0 );
    [ x_1( k, j) ]  = opd( out_1 );
    [ t_1( k, j) ]  = opd( out_2 );
    for i=j+1:1:N,
```

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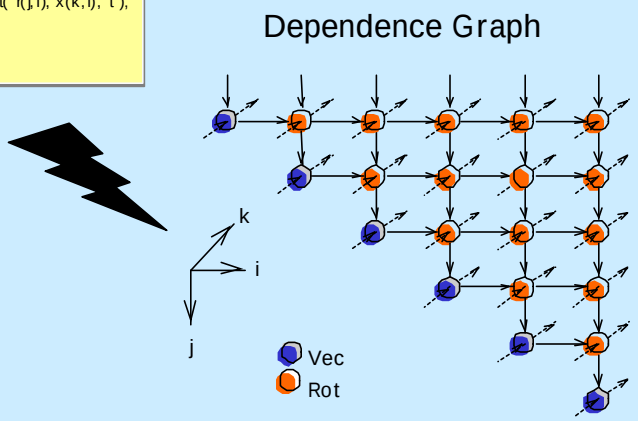
Dependence Graph

```
for k = 1:1:K,
  for j = 1:1:N,
    [r(j,j), x(k,j), t] = Vec( r(j,j), x(k,j) );
    for i = j+1:1:N,
      [r(j,i), x(k,i), t] = Rot( r(j,i), x(k,i), t );
    end
  end
end
```



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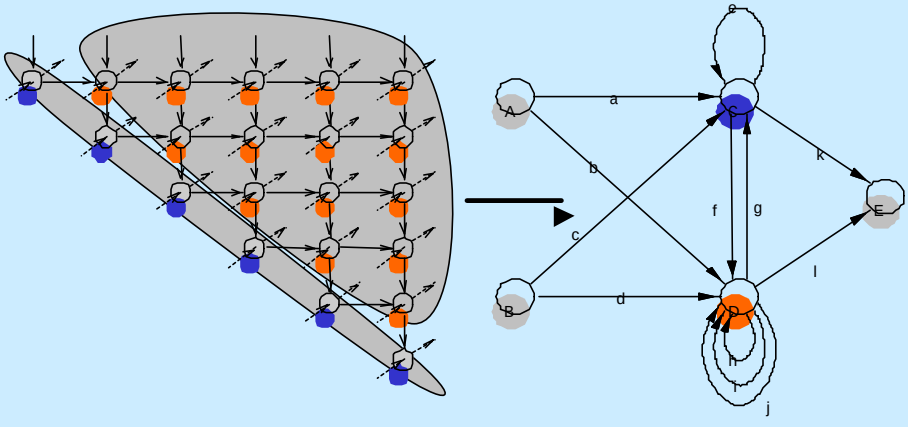
Step 2: DgParser



Polyhedral Reduced Dependence Graph

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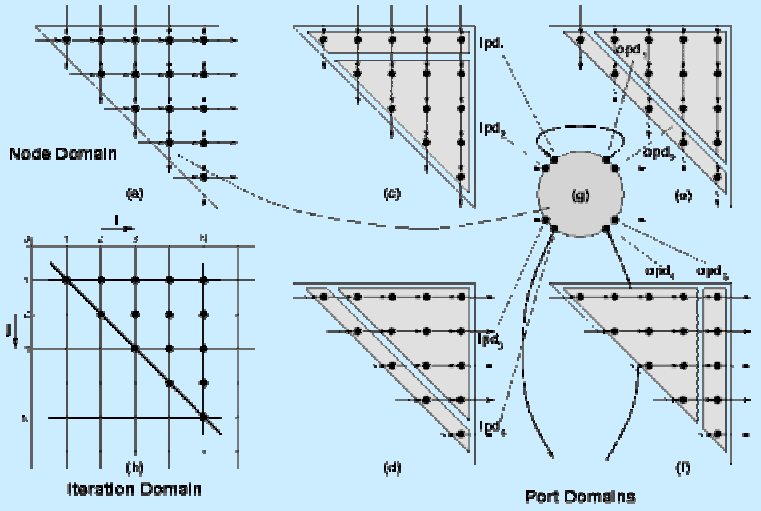
Example of Node and Port Domains



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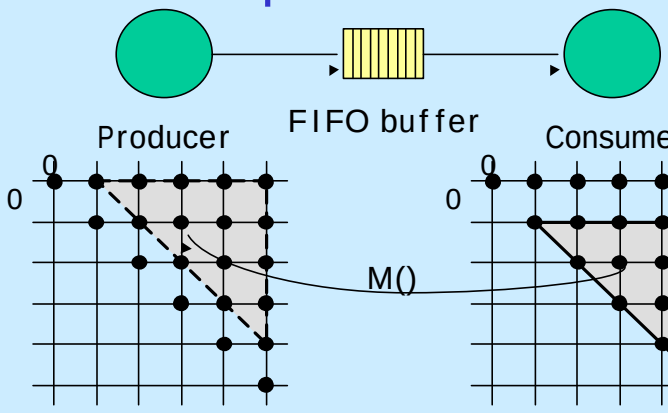
Step 3: PANDA



- Domain Reconstruction
- Domain Scanning
- Linearization

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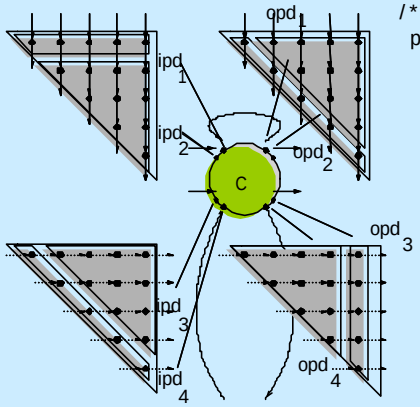
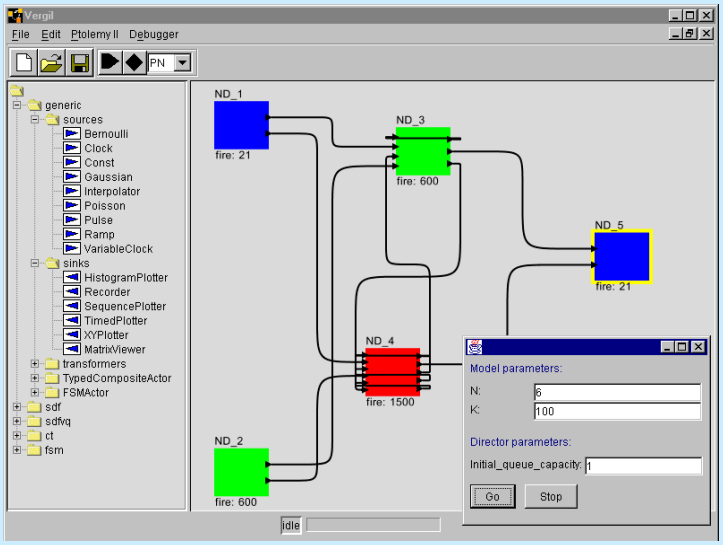
PN Model in Ptolemy II



Port Domains

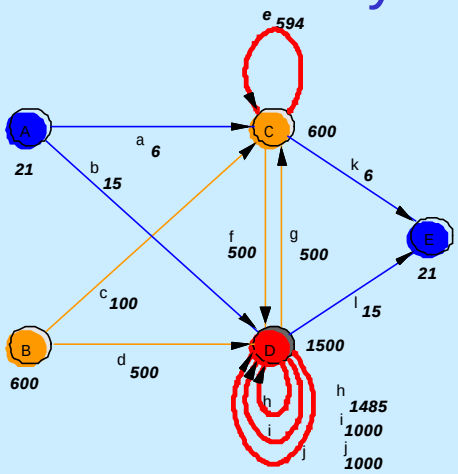
```
/** fire the actor. */
 public void fire() throws IllegalActionException {

   for ( int k = 1 ; k <= 1*K ; k += 1 ) {
     for ( int j = 1 ; j <= 1*N ; j += 1 ) {

       if ( k - 2 >= 0 ) { in_0 = RP_1.get(0);  }
       if ( k - 1 == 0 ) { in_0 =RP_2.get(0);   }
       if ( j - 2 >= 0 ) { in_1 = RP_3.get(0);   }
       if ( j - 1 == 0 ) { in_1 = RP_4.get(0);   }

       // Execute the function
       [out_0, out_1, out_2] = F.Vectorize(in_0, in_1);

       if ( K - k - 1 >= 0 ) { WP_1.send( out_0 );  }
       if ( -K + k == 0 ) { WP_11.send( out_0 );   }
       if ( N - j - 1 >= 0 ) { WP_10.send( out_2 );  }

     }
   }
 }
```


Ptolemy II, Simulation



Early Exploration

Workload Analysis



6 Antenna's
100 Updates

- Separation Communication/Computation
- Higher levels of granularity

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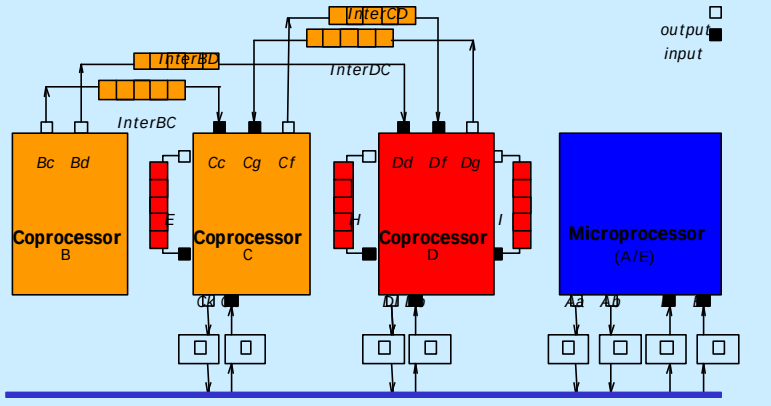
Exploration of Possible Architectures



Spade Environment

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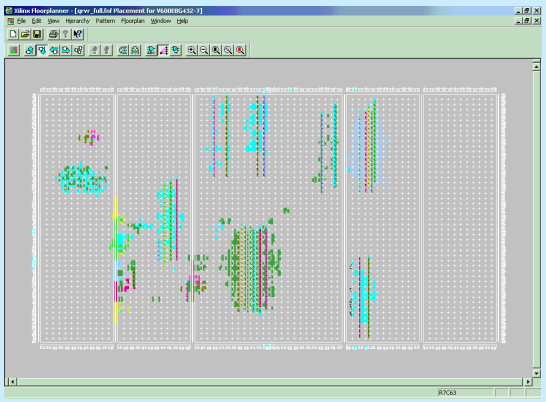
FPGA Hardware Realization



Xlilinx Virtex 600E

- Compaan 10 secs

2) Synthesis using Synplicity Synplify
1-2 minutes

3) Place and Route using Xilinx Design Manager 2-3 minutes

In cooperation with DERA, Farnborough, United Kingdom

DERA

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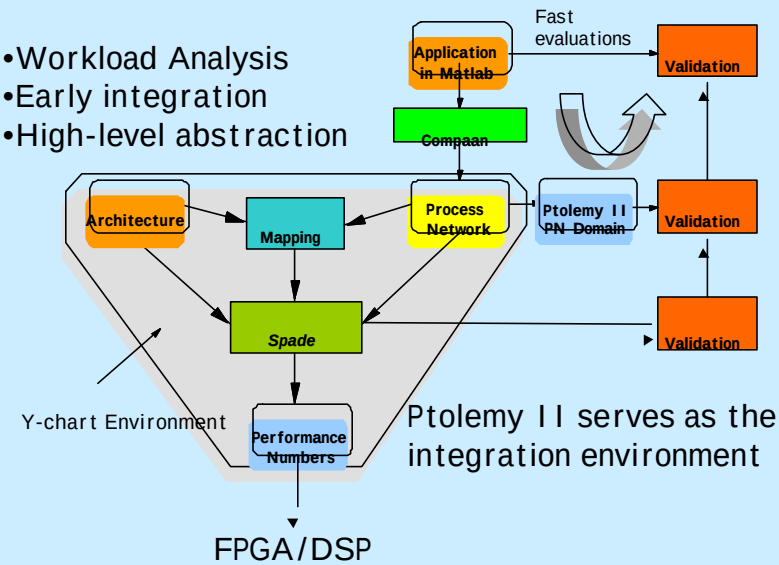
Y-chart

- Workload Analysis
- Early integration
- High-level abstraction



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