

Schedulers and Code Size

- For SDF semantics, use Ptolemy's **single-processor SDF schedulers** (**default, Joe's, SJS**) and **multi-processor SDF schedulers** (**Hu level, Sih dynamic level, Sih declustering**)
- **Code size** varies dramatically for different schedulers, especially for systems with large sample rate changes
- **Buffer size** also varies with different schedulers
- **Looping** requires indirect addressing of buffers, more overhead (buffer pointer, indirect addressing)
- **Tradeoff code size vs. buffer size**

```
/* Schedule 1 */
```

```
fire_star_A();  
fire_star_A();  
fire_star_A();  
fire_star_A();  
fire_star_A();
```

```
/* Schedule 2 */
```

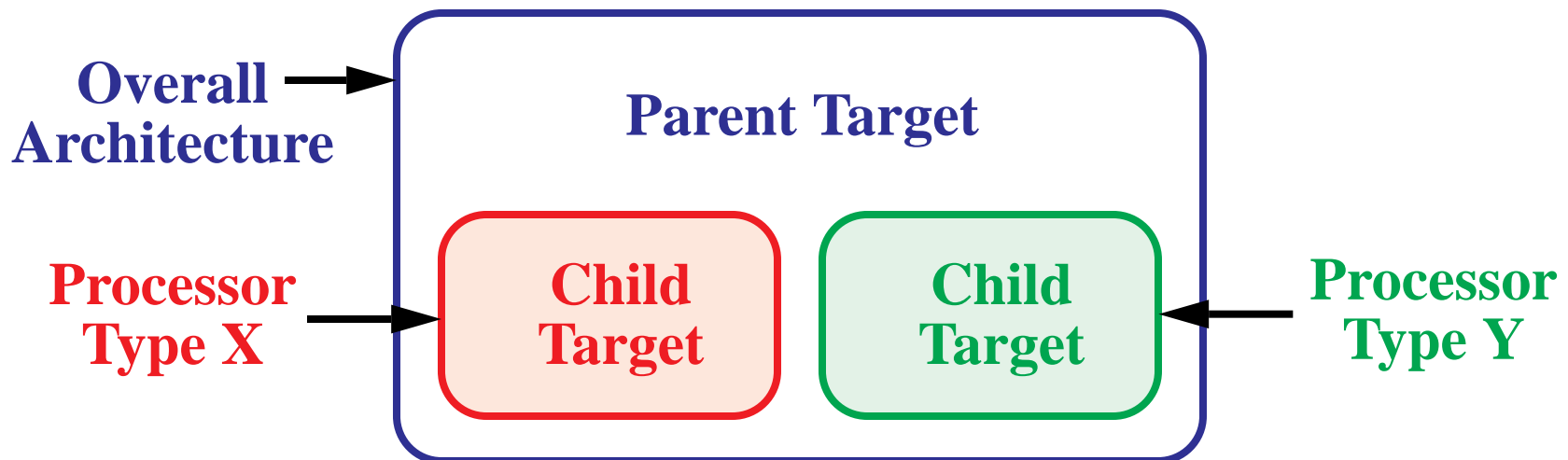
```
repeat(5) {  
    fire_star_A();  
}
```

Methods in Code Generation

- `generateCode()`
- `allocateMemory()`
- `codeGenInit()`
- `mainLoopCode()`
- `go()`
- `wrapup()`
- `frameCode()`
- `writeCode()`
- `compileCode()`
- `loadCode()`
- `runCode()`

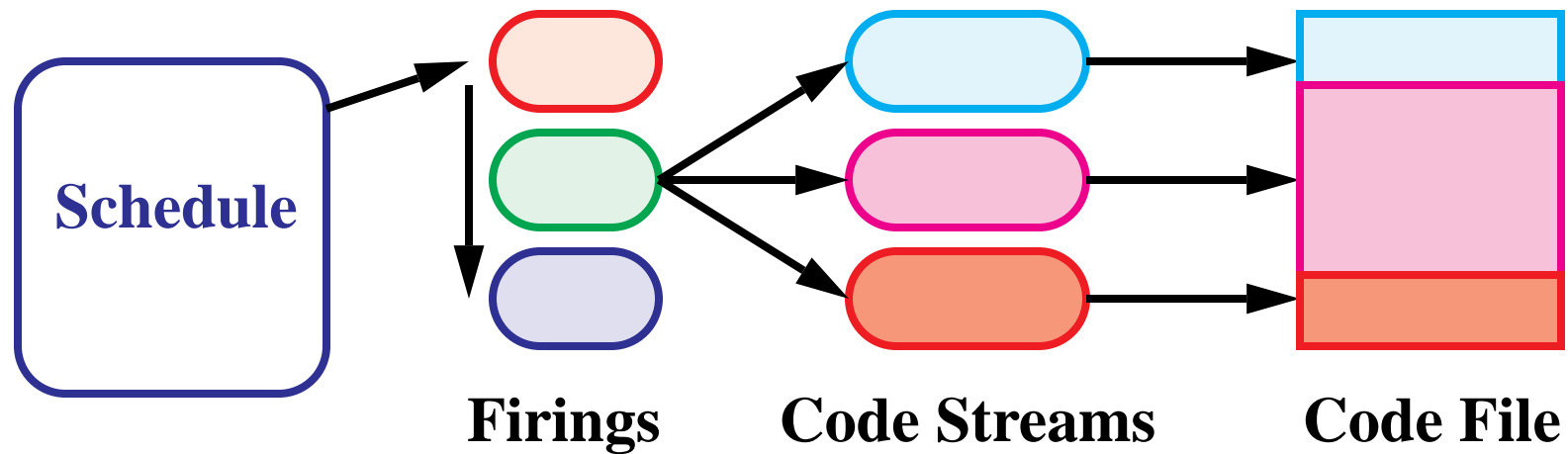
Multitargets

- Multiprocessor architectures
- Use targets hierarchically
- Heterogeneous architectures use heterogeneous targets
- Child targets generate code for their portion of the application
- Parent target coordinates all code generation and interaction with the architecture
- Special stars for synchronization between processors



Code Generation Targets

- **Targets correspond to architectures (single processor, multiprocessor, fully connected, shared bus, etc.)**
- **Multiple targets available for a single code generation domain**
- **Methods to generate schedule, fire individual stars**
- **Methods to generate individual code streams, assemble code streams into code file, generate code file**
- **Methods for compiling code, downloading code, running code**



Attributes

- **State Attributes**

- `A_GLOBAL, A_LOCAL`
- `A_SHARED, A_PRIVATE`
- `A_CONSTANT, A_NONCONSTANT`
- `A_SETTABLE, A_NONSETTABLE`
- `A_CIRC`
- `A_CONSEC`
- `A_MEMORY`
- `A_NOINT`
- `A_REVERSE`
- `A_SYMMETRIC`
- `A_ROM, A_RAM`

- **Porthole Attributes**

- `P_CIRC, P_SHARED, P_SYMMETRIC, P_NOINT`

Macros

- **Base CGStar Macros**

- `$ref(name), $ref(name, offset)`
- `$val(state-name)`
- `$size(name)`
- `$starName()`
- `$fullName()`
- `$starSymbol(name)`
- `$sharedSymbol(list, name)`
- `$label(name), $codeblockSymbol(name)`

- **Additional Macros**

- `$addr(name), $addr(name, offset)`
- `$ref(name, offset)`
- `$mem(name)`

Code Streams

- Distinguish among different sections of code (initialization, main loop, wrapup, declarations, procedures, functions, compiler directives)
- Methods related to `addCode()` to add code to specific code streams (e.g. `addProcedure()` to add code to `procedures` code stream)
- Variations of `addCode()` with arguments to control adding code to an argument code stream
- Check if same code has already been added, avoid redundant code for shared resources

Codeblocks

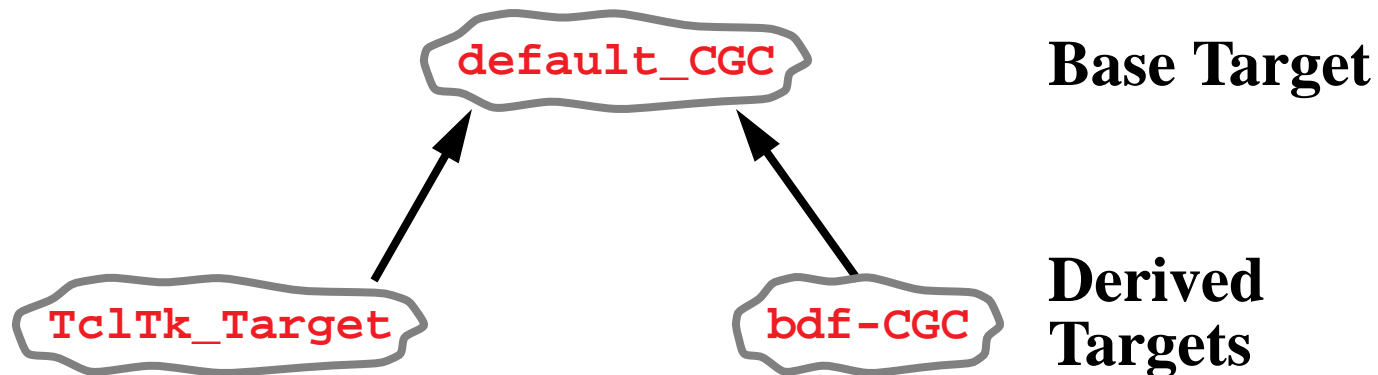
```
codeblock (std) {  
    $ref(output) = $ref(value);  
    $ref(value) += $val(step);  
}  
  
go { addCode(std); }
```

- A section of code which can be generated by a star
- Written in the output code language with interspersed **macros** to be expanded by preprocessing
- Referred to by an identifying name (**std**)
- Added to output code with **addCode()** or related methods
- Decision-making during star firing for conditional code generation

Elements of Code Generation Stars

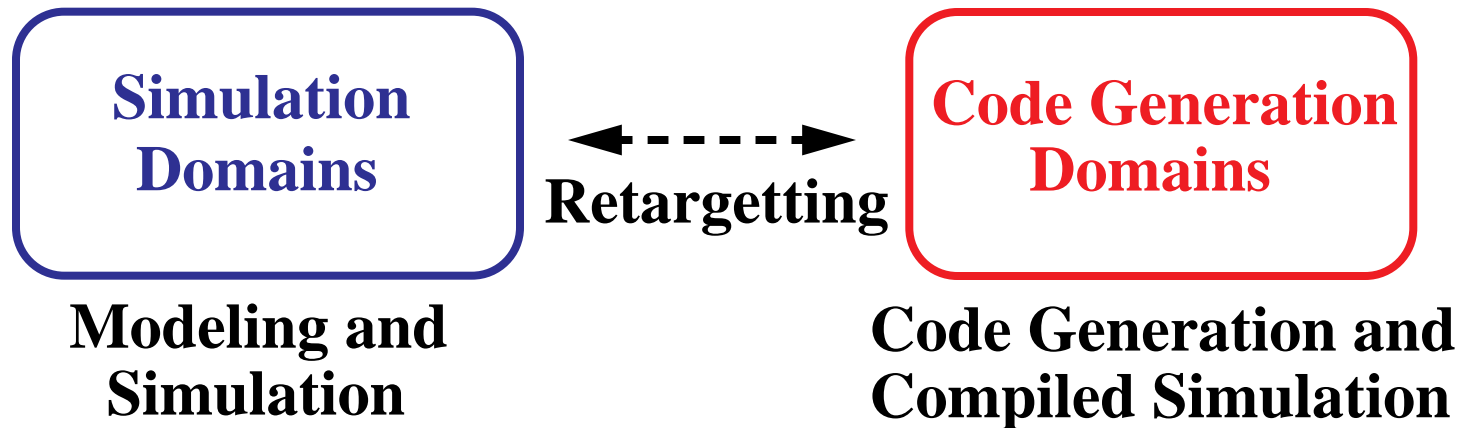
- Similar to simulation stars: `setup()`, `go()`, `wrapup()` methods
- Additional methods: `initCode()`, `execTime()`
- `setup()`: Initialize local variables and states, called before schedule is generated
- `initCode()`: Generate initialization code before the main loop, procedure declaration code outside the main loop, called after schedule is generated
- `go()`: Generate code in the main loop for one firing
- `wrapup()`: Generate code after the main loop
- `int execTime()`: Returns execution time of one firing in main loop in processor cycles or instruction steps; Used primarily in parallel scheduling

Code Generation Classes



- **Domains correspond to particular languages (C, assembly, Silage, VHDL)**
 - Default target
 - Supported star type
- **Targets correspond to different target architectures**
 - Derived from base class target
 - Control scheduling, compiling, assembling, downloading code
 - Multiprocessor architectures: task partitioning and synchronization

Relationships Between Domains



- **CG domain for comment generation, test schedulers**
- **Domains derived from CG for language-specific code generation**
- **Dataflow semantics supported, other semantics possible**
- **CG kernel: processor-independent actions**
 - allocate memory for buffers, constants, tables
 - generate symbols, labels

Generate System Descriptions for Design Tools

The image displays a design tool interface with three main components:

- Schematic View:** A diagram showing a 'RampInt' block connected to a 'FIRInt' block. The 'FIRInt' block contains a summing junction and several delay elements.
- Design Analyzer:** A window showing the 'Schematic View' of the 'FIRIntTest' design. It includes a toolbar and a menu bar (Setup, File, Edit, View, Attributes, Analysis, Tools, Help). The main area shows a detailed schematic of the FIR filter implementation.
- Code Editor:** A window showing the HDL code for the 'FIRIntTest' design. The code is written in a hardware description language and includes comments and logic for the FIR filter.

```
Cluster: FIRIntTest_RampInt_0
-- Entity: FIRIntTest_RampInt_0
-- Date:   Thu Jul 13 18:31:47 1995
-- Target: Synopsys-FPGA
-- Macrocell: FIRIntTest

Cluster: FIRIntTest_RampInt_0
entity FIRIntTest_RampInt_0 is
    port(
        FIRIntTest_RampInt5_output_0: IN INTEGER range 0 to 15;
        FIRIntTest_RampInt5_value_1_in: IN INTEGER range 0 to 15;
        FIRIntTest_RampInt5_value_2_in: IN INTEGER range 0 to 15;
    );
end FIRIntTest_RampInt_0;

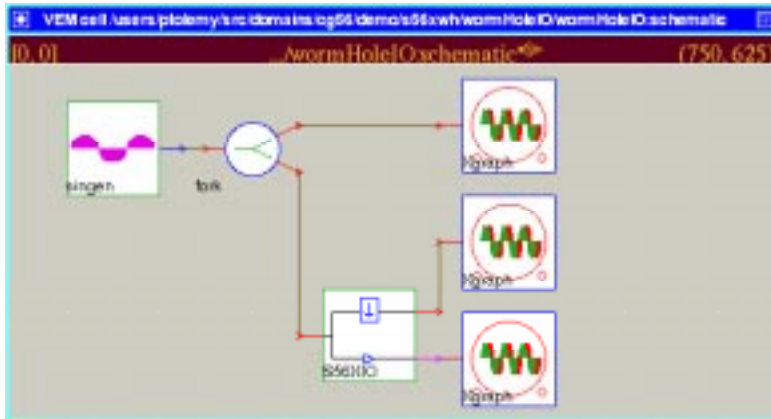
architecture Behavior of FIRIntTest_RampInt_0 is
begin
    process
    c
        FIRIntTest_RampInt5_value_1_in
    c
        variable FIRIntTest_RampInt5_value_2: INTEGER range 0 to 15;
begin
    FIRIntTest_RampInt5_value_2 := FIRIntTest_RampInt5_value_1_in;
    FIRIntTest_RampInt5_output_0 := FIRIntTest_RampInt5_value_2;
    FIRIntTest_RampInt5_value_2 := FIRIntTest_RampInt5_value_1 + 1;
    FIRIntTest_RampInt5_value_2 := FIRIntTest_RampInt5_value_2;
end process;
end Behavior;

-- Cluster: FIRIntTest_FIRInt_0
entity FIRIntTest_FIRInt_0 is
    port(
        FIRIntTest_FIRInt5_output_0: IN INTEGER range 0 to 15;
        FIRIntTest_FIRInt5_output_1: IN INTEGER range 0 to 15;
        FIRIntTest_FIRInt5_output_2: IN INTEGER range 0 to 15;
        FIRIntTest_FIRInt5_output_3: IN INTEGER range 0 to 15;
        FIRIntTest_FIRInt5_output_4: IN INTEGER range 0 to 15;
    );
end FIRIntTest_FIRInt_0;

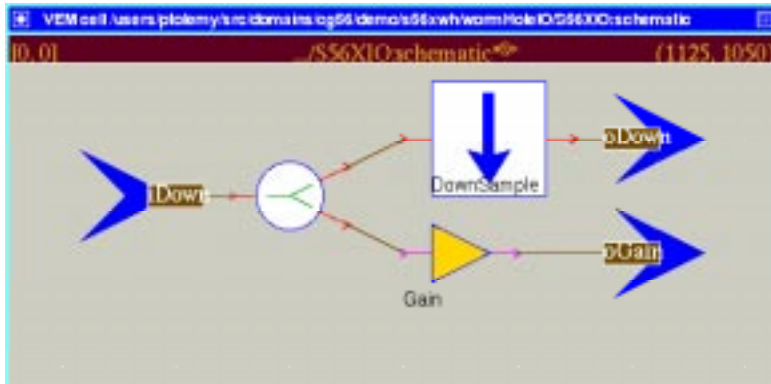
-- Information about the HDL Project and the goals, top Edb Exp.
```

- **Generate system descriptions for processing by other design tools (Silage-->Hyper, VHDL-->Synopsys)**
- **Domains: Silage, VHDLF, VHDLB**

Generate Code for Co-simulation



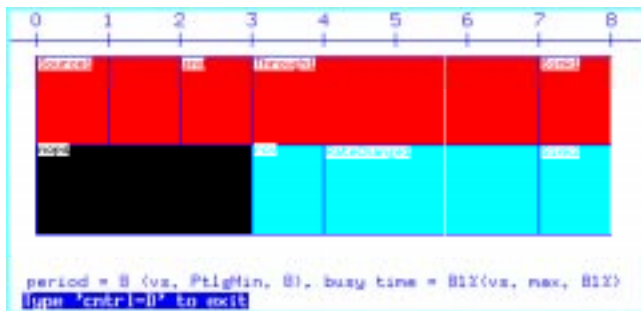
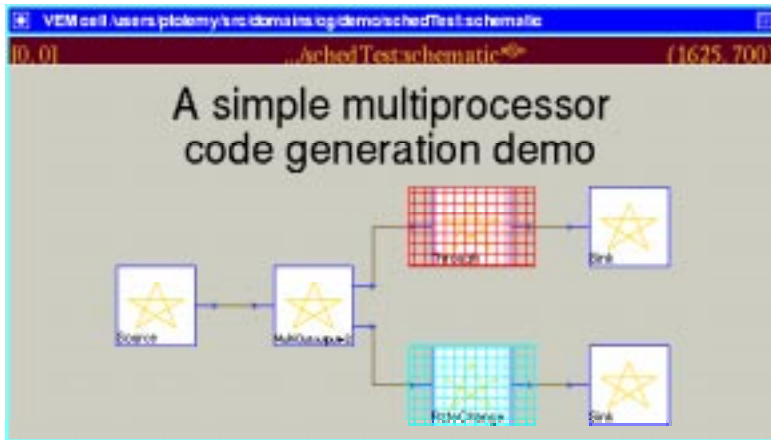
Top-level SDF system



CG56 subsystem

- **Generate code for co-simulation between Ptolemy and code running on hardware connected to a workstation**
- **Targets: S-56X, S-56XWH**

Test Multiprocessor Schedulers

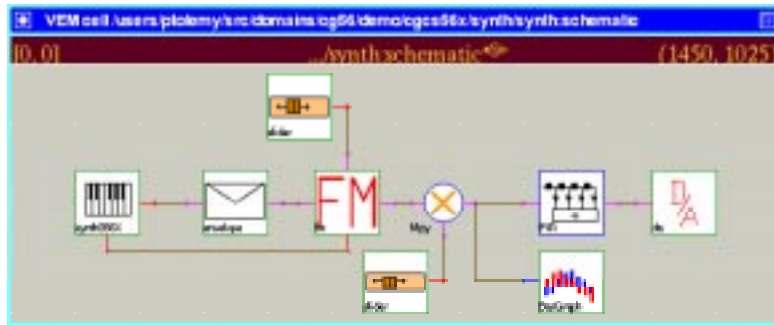


Parameter	Value
directory:	HOMEPTOLEMY_SYSTEMS
file:	
display:	YES
compile:	NO
run:	NO
npocs:	2
inheritProcessors:	NO
seedTime:	1
useStarOverProc:	NO
manualAssignment:	NO
adjustSchedule:	NO
childType:	default-CG
resources:	
refTimeScales:	1
ganttChart:	YES
logFile:	stdout-
serializedComm:	NO
ignoreIPC:	NO
overlapComm:	NO
useCluster:	YES
Use multiple schedulers?:	NO

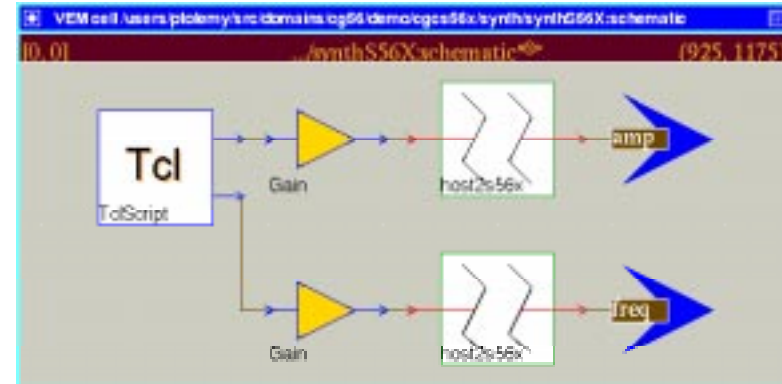
- **Domains: CG; CGTargets: FullyConnected, SharedBus**
- **Other Targets: unixMulti_C, MultiSim-56000**

Generate Code for Heterogeneous Architectures

Top-level CG56 system



CGC subsystem



↓

56000 Code

**Run on processor
on S-56X card**

↓

C Code

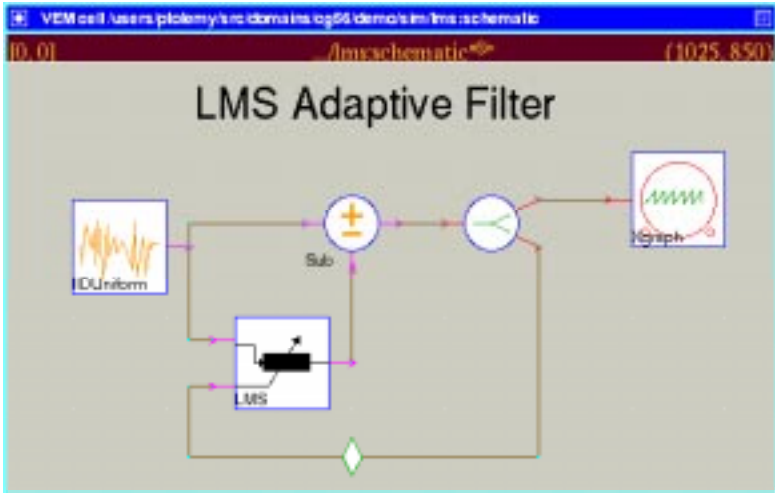
Run on SparcStation

↔

Target sets up communication

- **Domains: CG56**
- **Targets: CGC-S56X**

Generate Code for Special-Purpose Processors



Generated Code

```
...
org p1
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org p2
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org p3
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org p4
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org p5
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org p6
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```

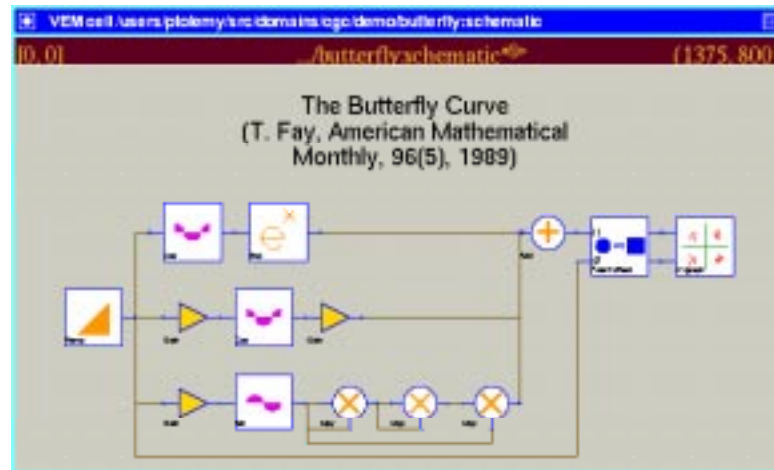
Compiler

Processor Simulator

Processor Architecture

- Domains: CG56, CG96, Sproc

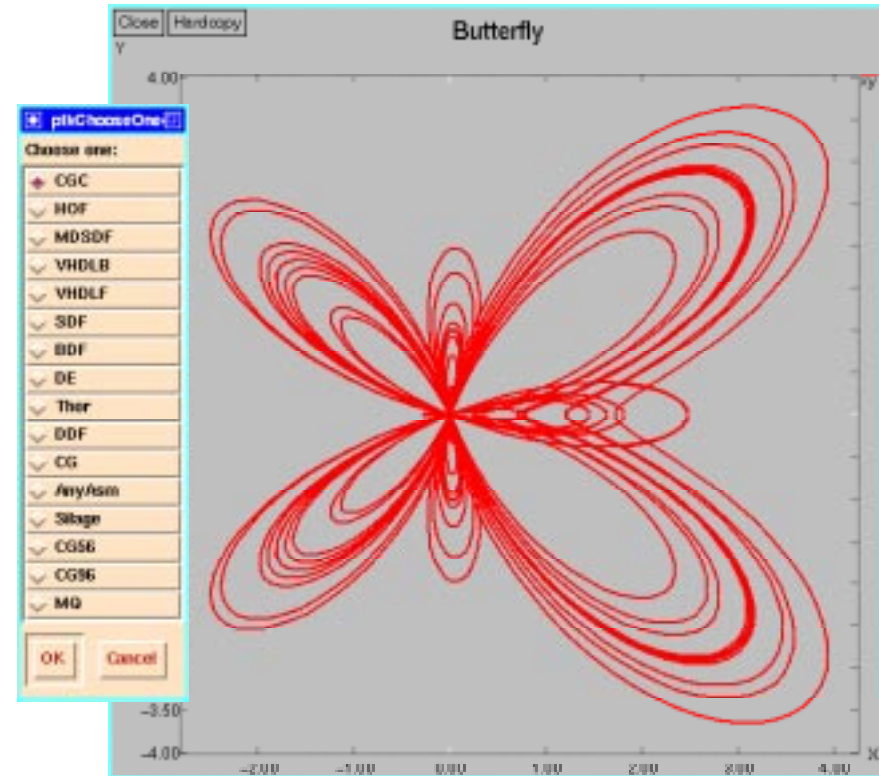
Generate Standalone Simulation Programs



```

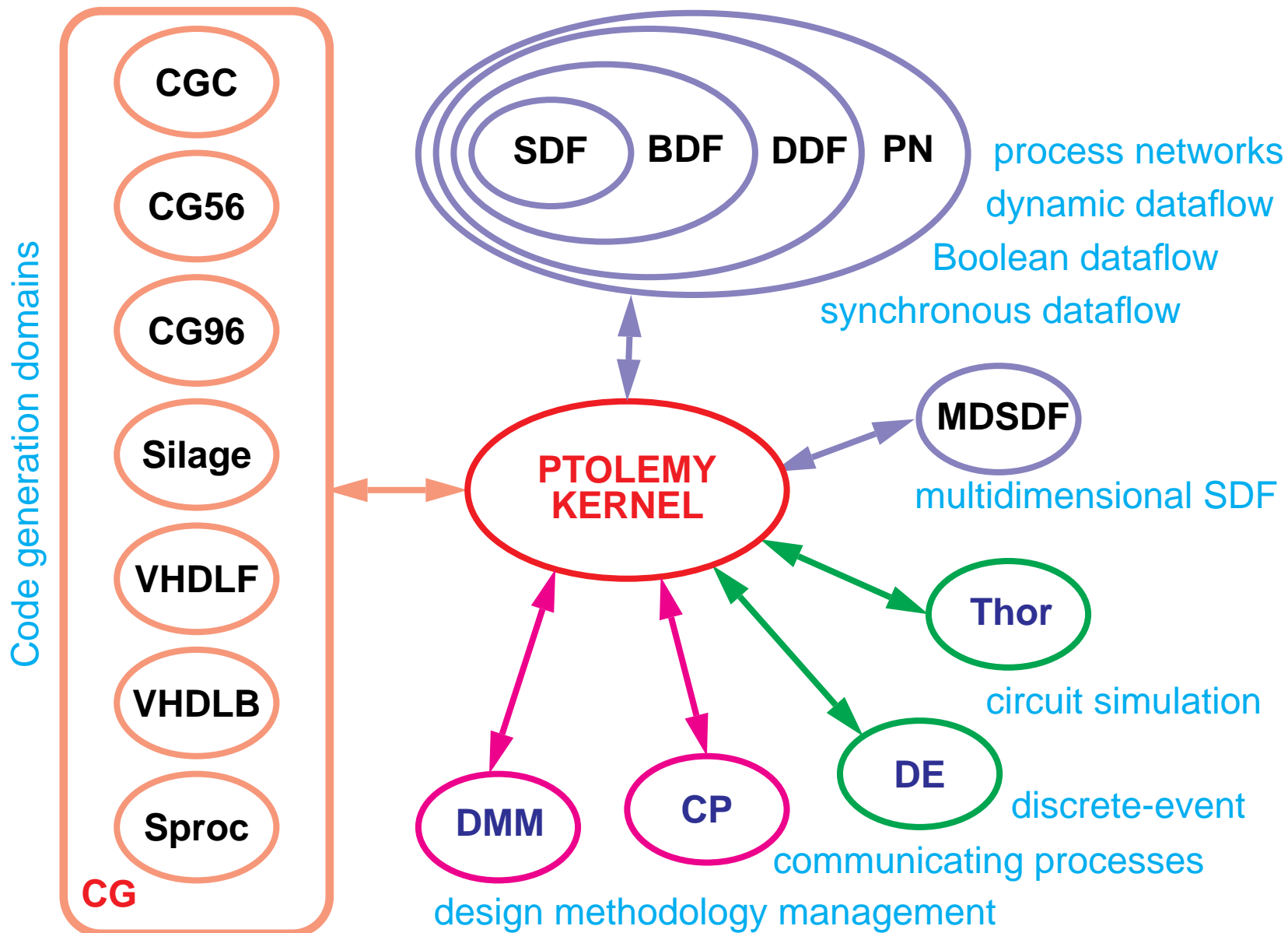
...
File: /home/pls/p1/ptolemy/ptolemy2/domains/cgc/butterfly/schematic
File: /home/pls/p1/ptolemy/ptolemy2/libraries/cgc/cgc
File: /home/pls/p1/ptolemy/ptolemy2/libraries/cgc/cgc/cgc
...

```



- Retarget from SDF or build from scratch in CGXXX
- Run on workstation independent of Ptolemy
- Recompile code to run on other platforms

Domains in Ptolemy



Outline

- **Applications of Code Generation**
- **Relationships Between Domains**
- **Code Generation Classes**
- **Elements of Code Generation Stars**
 - **Codeblocks**
 - **Code Streams**
 - **Macros**
 - **Attributes**
- **Code Generation Targets**
- **Multitargets**
- **Methods in Code Generation**
- **Schedulers and Code Size**

Code Generation Concepts



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