



Ptolemy Miniconferences

Edward A. Lee

Robert S. Pepper Distinguished Professor

Ninth Biennial Ptolemy Miniconference

February 16, 2011

Berkeley, CA, USA



Ptolemy Project

February, 2011

Staff:

- Christopher Brooks
- Edward A. Lee (PI)
- Stavros Tripakis
- Mary P. Stewart

Postdocs:

- Patricia Derler
- Slobodan Matic
- Eleftherios Matsikoudis
- Jan Reineke

Grad Students:

- Ilge Akkaya
- Dai Bui
- Shanna-Shaye Forbes
- Ben Lickly
- Isaac Liu
- Chris Shaver
- Jia Zou
- Mike Zimmer

Visiting Scholars:

- Hugo Andrade
- Janette Cardoso
- John Eidson



Photo by Chamberlain Fong



The 1st Biennial Ptolemy Miniconference: 1995

The Ptolemy Project

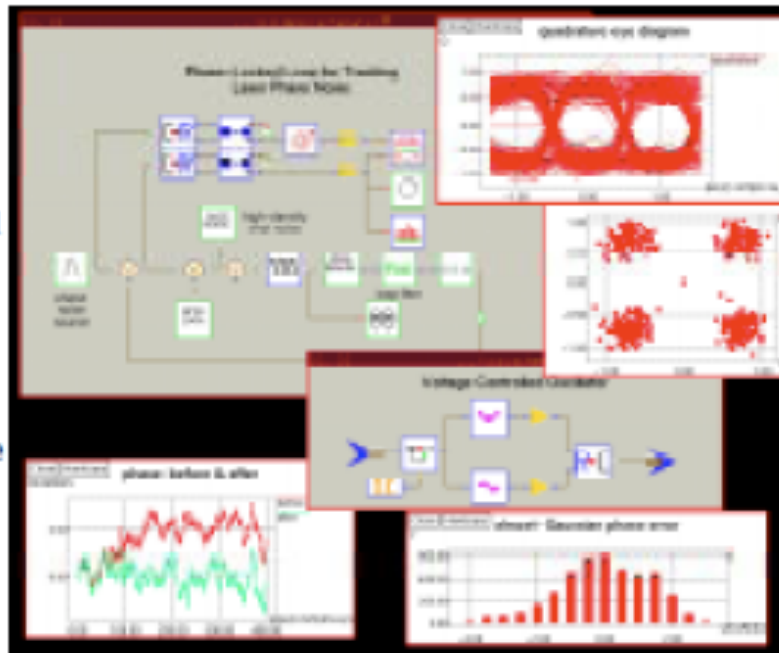


Shuvra Bhattacharyya
Joseph T. Buck
Wan-Teh Chang
Brian L. Evans
Steve X. Gu
Sangjin Hong
Christopher Hylands
Asawaree Kalavade
Alan Kamas
Allen Lao
Bilung Lee
Edward A. Lee
David G. Messerschmitt
Praveen K. Murthy
Thomas M. Parks
José Luis Pino
Farhana Shiekh
S. Sriram
Juergen Teich
Warren W. Tsai
Patrick J. Warner
Michael C. Williamson

System-Level Design of Signal Processing Systems

Ptolemy Research

- Design complexity management.
- Visual, algorithm-level system design.
- Formal methods for dataflow systems.
- Programming language semantics.
- Software and hardware synthesis.
- Parallel architectures, partitioning, and scheduling.



This highly multidisciplinary project addresses system-level design and implementation of signal processing systems.

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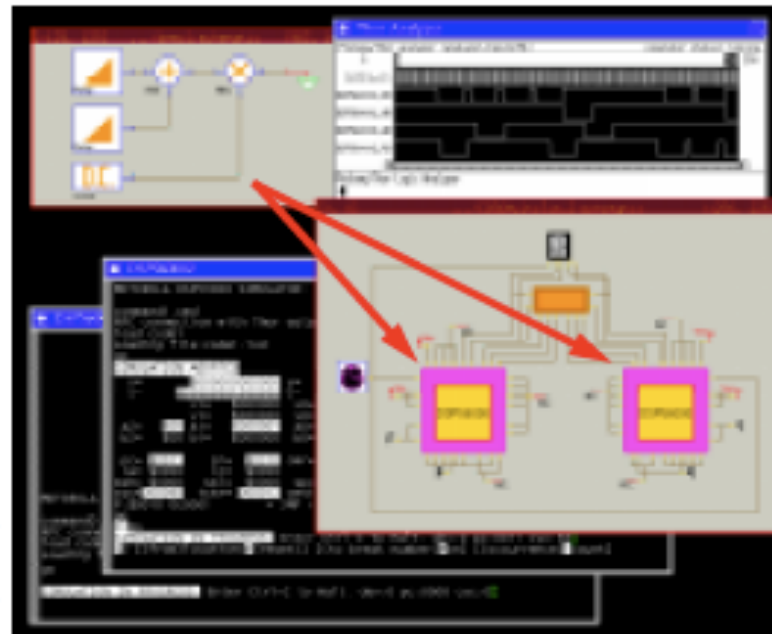
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Implementation of Signal Processing Systems

Hardware/ Software Synthesis

- Design of heterogeneous embedded systems.
- Real-time systems.
- Synthesis of software from dataflow graphs.
- System-level hardware design.
- Cosimulation of hardware and software.
- Codesign of hardware and software.



The design philosophy in Ptolemy is heterogeneous, allowing for effective use of specialized design tools within a general system-level design environment.

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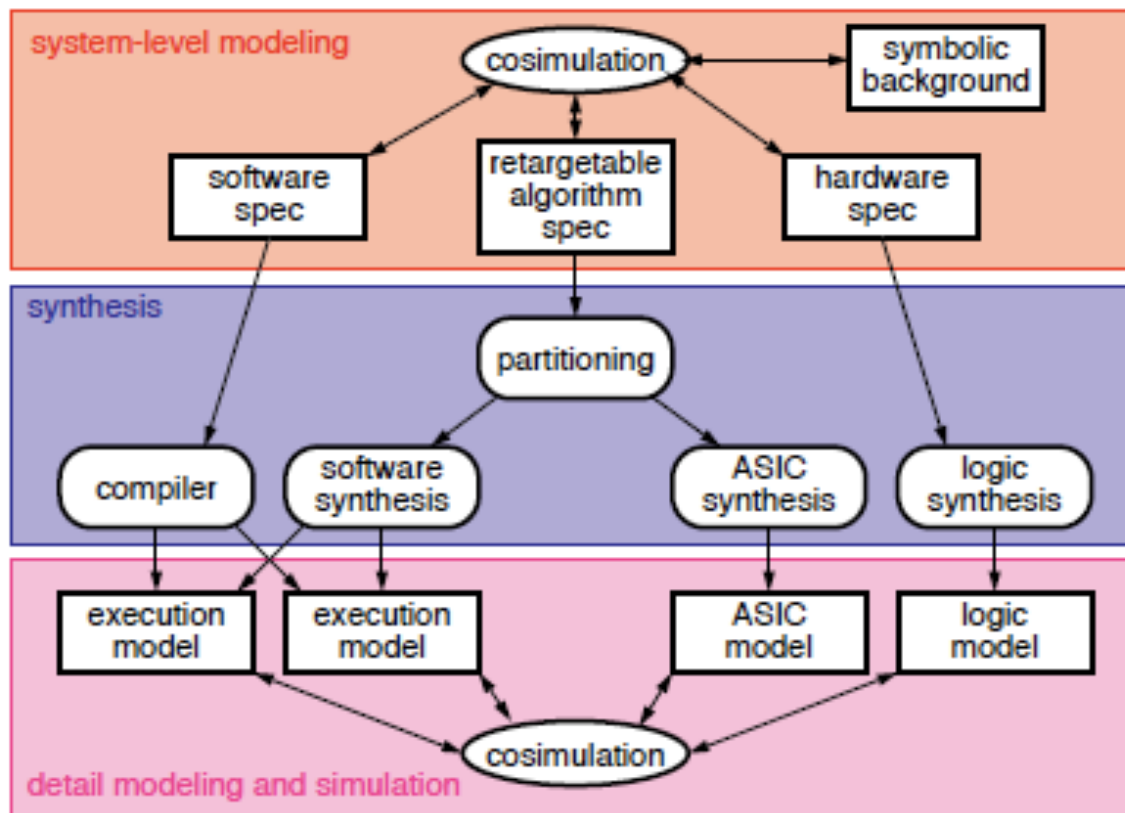
The Ptolemy Project



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Heterogeneity in System-Level Design



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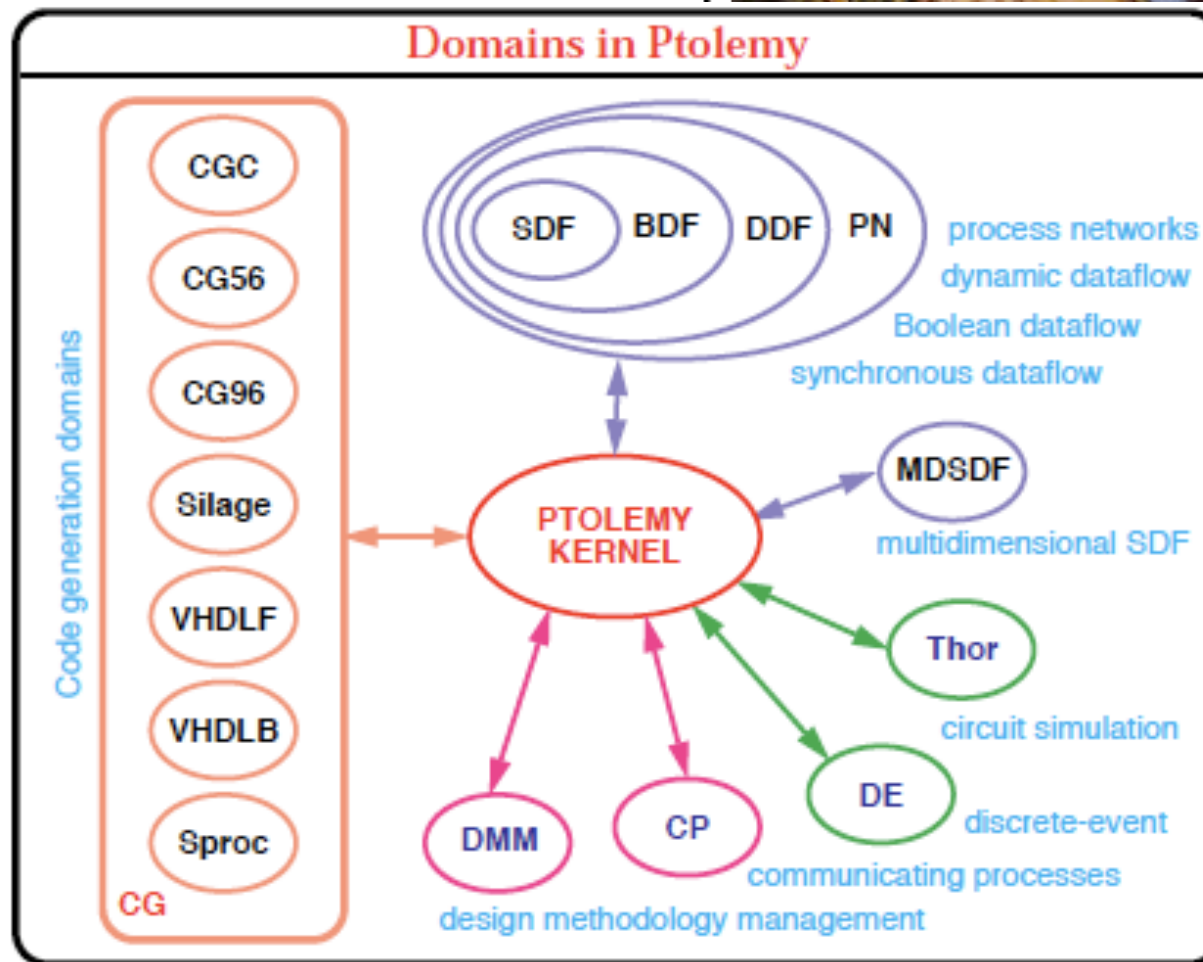
The Ptolemy Project



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Domains in Ptolemy



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Patrick J. Warner
Michael C. Williamson

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Where to From Here?

- Real-time scalable computing.
- Scalable embedded systems design.
- Design migration from abstract to concrete.
- Formal methods based on partial orders.
- Hybrid systems: combining FSM with dataflow.
- Modeling and analysis of random systems.
- Design of nondeterminate systems.
- Complexity management.
- Design visualization and documentation.
- Partial evaluation and incremental compilation.
- Models for back-end signal interpretation.
- Heterogeneous scheduling.

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Organizational

Staff

Diane Chang, administrative assistant
 Kevin Chang, programmer
 Christopher Hylands, programmer analyst
 Edward A. Lee, professor and PI
 Mary Stewart, programmer analyst

Postdocs

Praveen Murthy
 Seehyun Kim
 Raja Nagarajan
 John Reekie
 Dick Stevens (on leave from NRL)

Students

Sunil Bhawe
 Cliff Cordeiro
 John Davis
 Stephen Edwards
 Ron Galicia
 Mudit Goel
 Michael Goodwin
 Luis Gutierrez
 Bilung Lee

ilp_overview.doc

UNIVERSITY OF CA

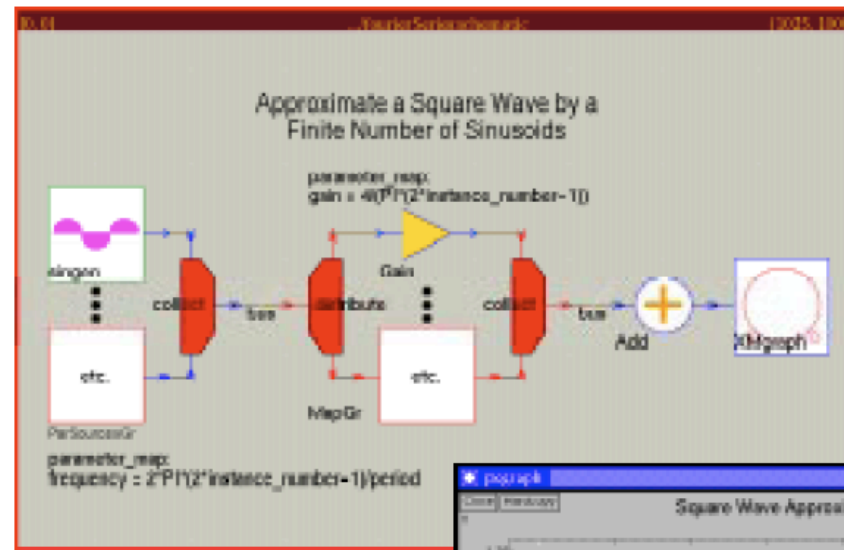
Michael C. Williamson
 Yuhong Xiong

Key Outside Collaborators

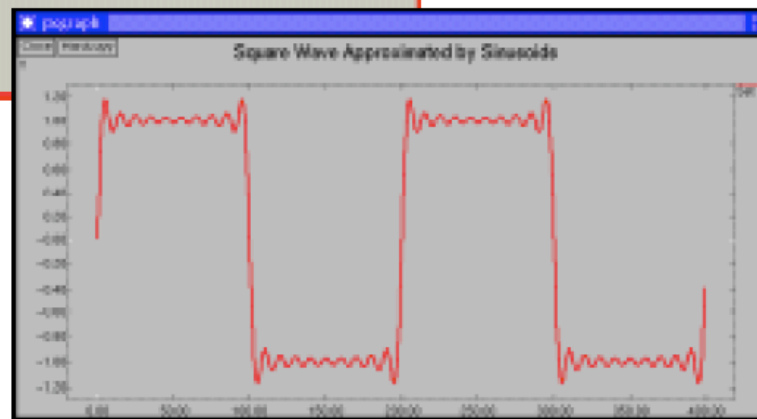
Shuvra Bhattacharyya (Hitachi)
 Joseph T. Buck (Synopsis)
 Brian L. Evans (UT Austin)
 Soonhoi Ha (Seoul N. Univ.)
 Tom Lane (SSS)
 Thomas M. Parks (Lincoln Labs)
 José Luis Pino (Hewlett Packard)

The 2nd Biennial Ptolemy Miniconference: 1997

Visual Design



- Formal properties.
- Scalability.
- Scheduling.
- Partitioning.



ilp_overview.doc

© 1997, p. 10 of 15

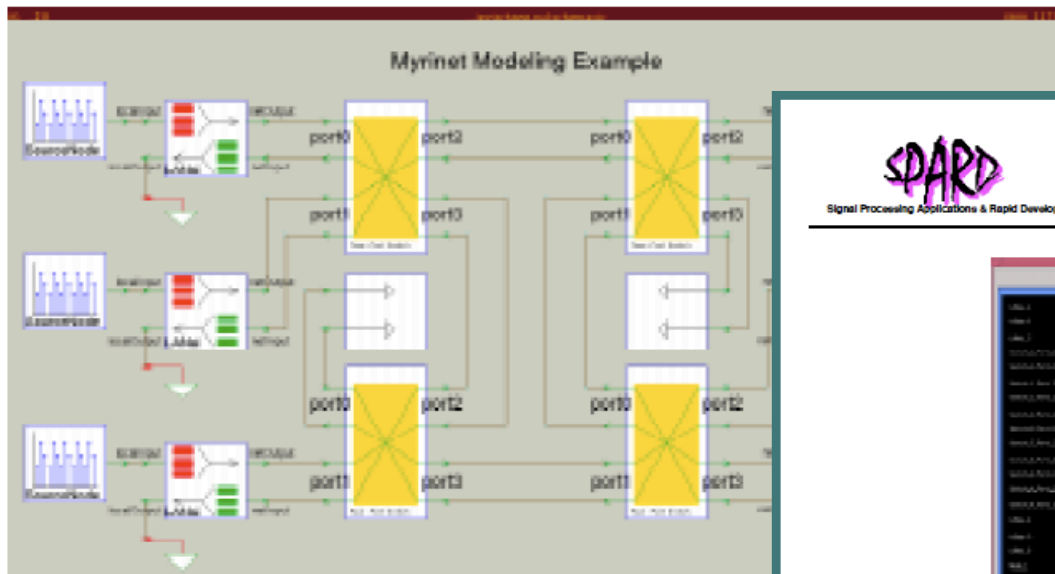
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The 2nd Biennial Ptolemy Miniconference: 1997



Simple Myrinet Modeling Example



Simple Myrinet Modeling Example



Modeling Results for Simple Example



Gantt Tool Display of Simple Myrinet Modeling Example

- **Yellow:** start-up latency
- **Blue:** normal transmission/reception
- **Green:** processing of data on Node
- **Orange:** origin of contention, one or more packets queued in the switch
- **Red:** propagating effect of switch contention down current data path

High-Performance Scalable
Computing (HPSC) modeling
by Sanders, a Lockheed-
Martin Company.



The 2nd Biennial Ptolemy Miniconference: 1997

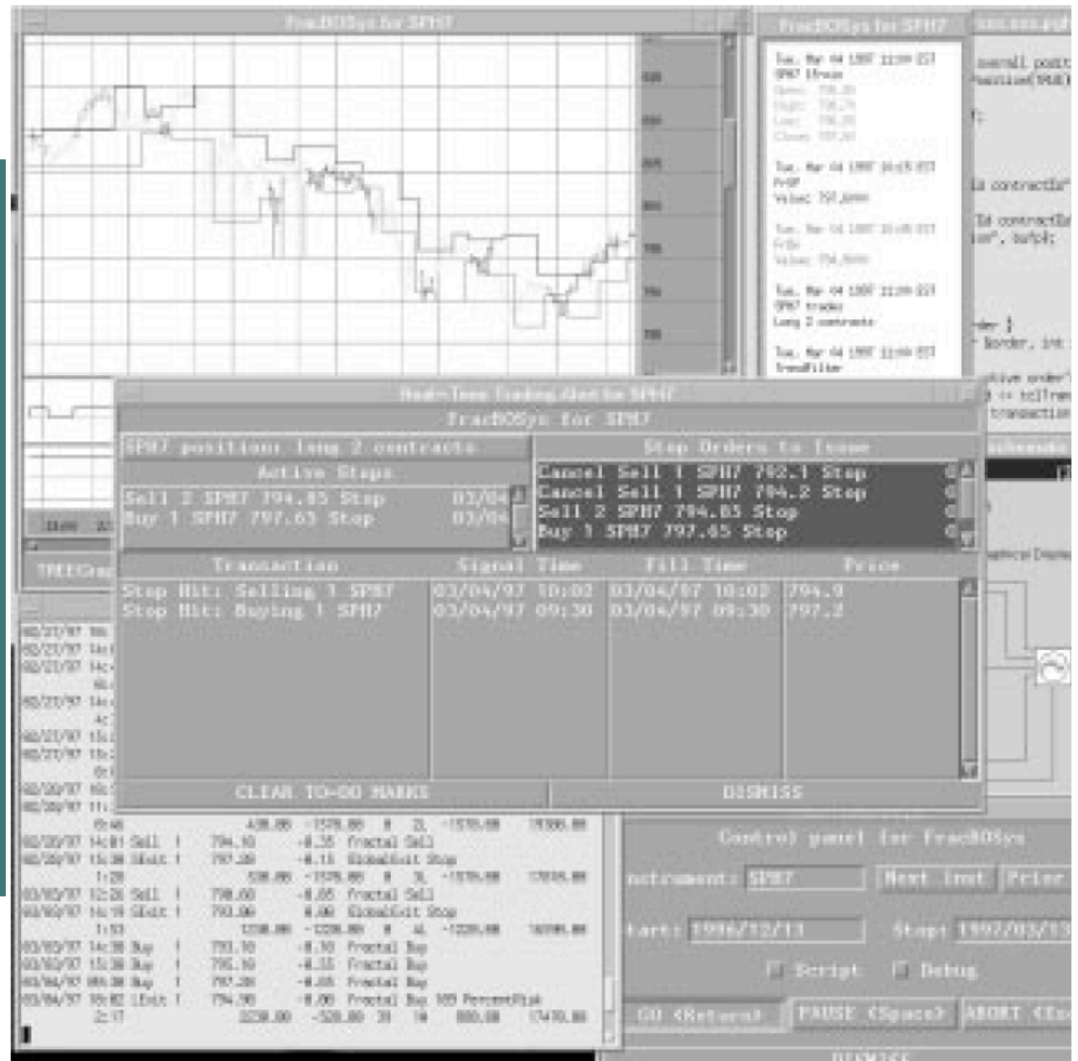
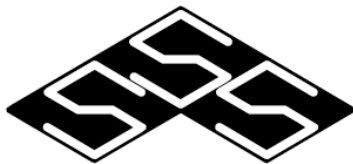
Live trading
example

Applications of Ptolemy in Securities Trading

or,
Playing the Markets with Ptolemy

Tom Lane

Structured Software Systems, Inc.





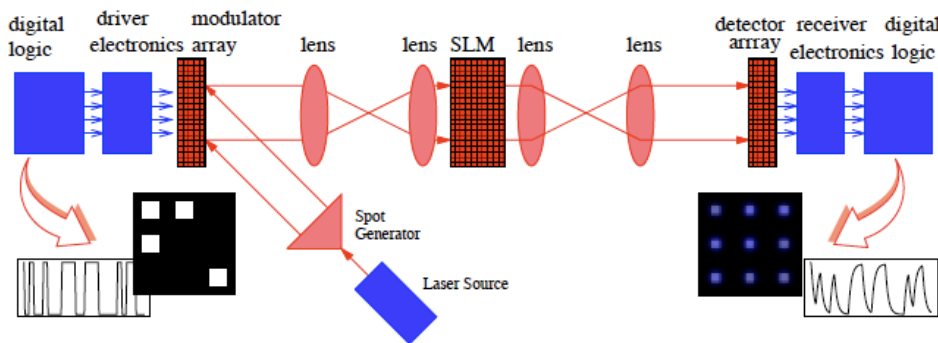
The 2nd Biennial Ptolemy Miniconference: 1997

Overview

Chatoyant is a computer aided design tool for the design of *Free Space Optoelectronic Information processing (FSOI) Systems*.

Simulation - Analysis - Synthesis - Interface

Enable the modeling of FSOI systems without costly prototyping



chatoyant



Modeling Free Space Optoelectronic Systems Using Ptolemy



Steven P. Levitan
Donald M. Chiarulli

Tim P. Kurzweg
Mark A. Rempel

Departments of
Electrical Engineering &
Computer Science
steve@ee.pitt.edu
http://kona.ee.pitt.edu/steve
University of Pittsburgh

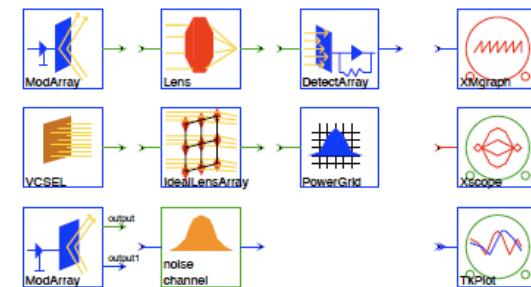
Philippe J. Marchand
Chi Fan

Fredrick B. McCormick

Department of Electrical &
Computer Engineering
pmarchand@ucsd.edu
http://soliton.ucsd.edu
University of California, San Diego

Funding: National Science Foundation- MIP-9421777

Chatoyant Stars in Ptolemy



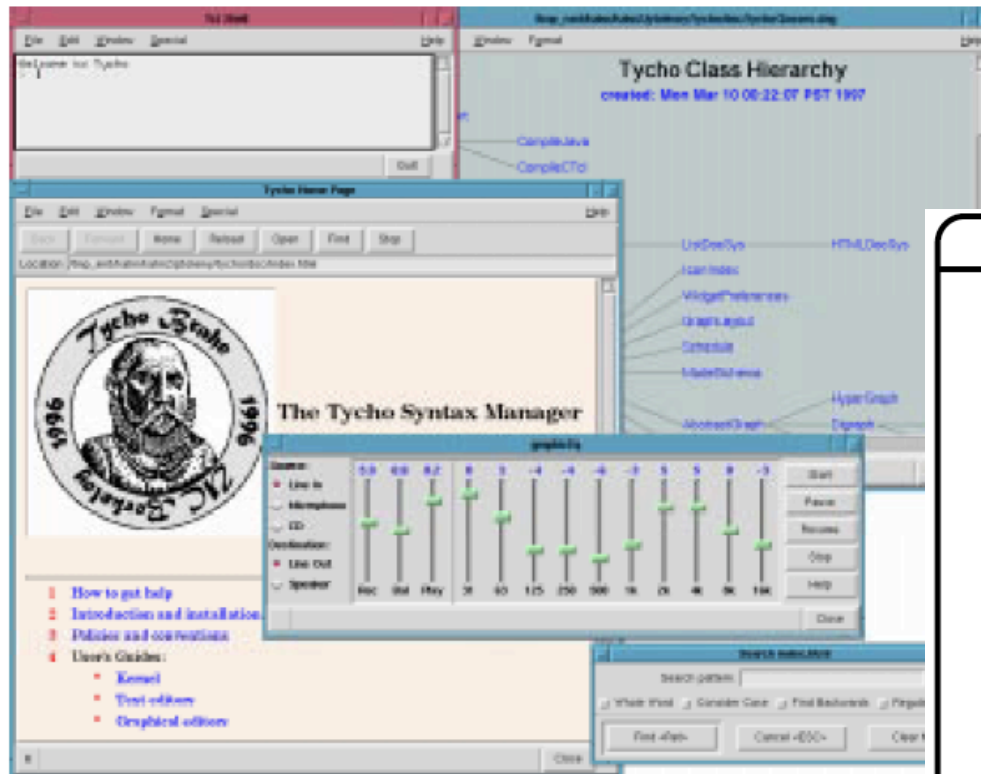
Modulators	Detectors	Lenses	Lenslets
Area	Detector Size	Focal Length	Focal Length
Spacing	Detector Spacing	Diameter	Diameter
Lambda	Distance	Distance	Distance
Footsize	x, y offsets	x, y offsets	x, y offsets
Filename	Radius of Integration		Spacing
Gauss/Ray	R, C, A		Number

chatoyant



The 2nd Biennial Ptolemy Miniconference: 1997

Tycho (1)



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Tycho



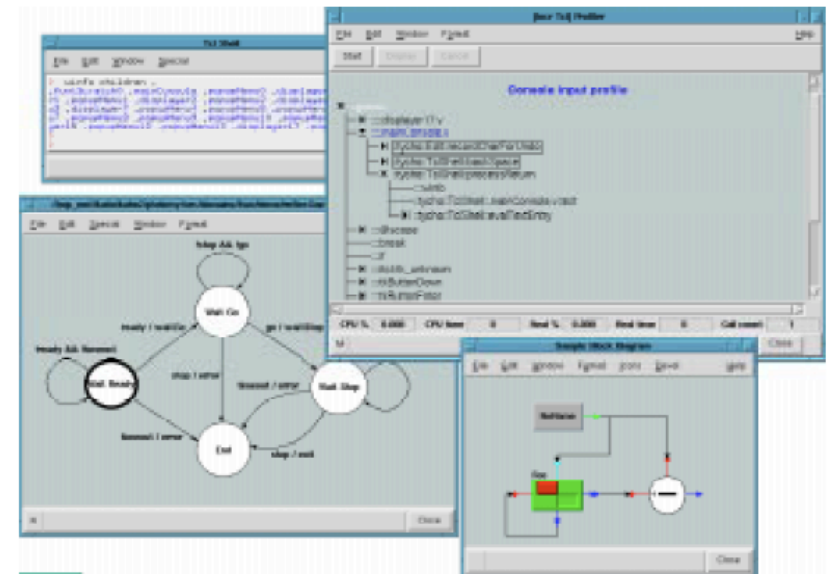
Christopher Hylands
Edward A. Lee
H. John Reekie

Contributors:

Kevin Chang
Wan-Teh Chang
Cliff Cordeiro
Wei-Jen Huang
Joel King
Farhana Sheikh
Mario Jorge Silva

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Tycho (2)



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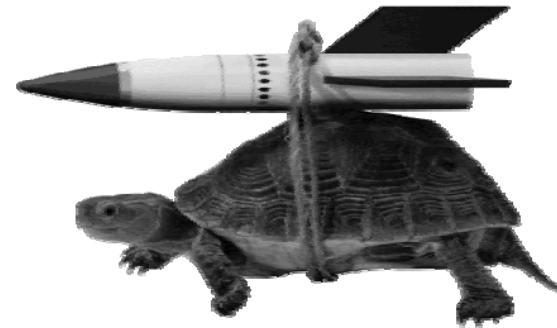
3rd Biennial
PtConf 1999

The switch to Ptolemy II

Ptolemy Classic vs Ptolemy II

C++	Java
Mature platform	Experimental
Does code generation	All Java (now)
Monolithic tool	Modular packages
Standalone	Networked
Sequential	Multi-threaded
GUI-centric	Applet-centric
Ad-hoc development	Good software practice
Dynamically linked	Reflective
Astronomical lexicon	Boring lexicon

Modeling in Java ?!?!?!?!?



- Choosing the best modeling technique can have a far bigger impact than using a faster modeling tool.
- Mixing modeling techniques permits multi-domain modeling using the best available modeling techniques.
- Threads, objects, and UI infrastructure helps with both.
- Network integration of Java promotes sharing of modeling methods.
- Java performance and infrastructure is rapidly improving.

The Ptolemy Project Heterogeneous Modeling and Design



Principal Investigator
Edward A. Lee

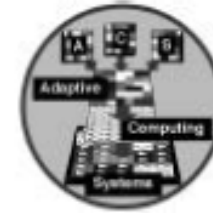
Staff
Jennifer Basler
Christopher Hylands
Mary P. Stewart

Postdocs/Researchers
Bart Kienhuis
James Lundblad
John Reekie

Students
John Davis, II
Ron Galicia
Mudit Goel
Bilung Lee
Michael Leung
Jie Liu
Xiaojun Liu
Lukito Muliadi
Steve Neuendorffer
Neil Smyth
Jeff Tsay
William Wu
Yuhong Xiong



3rd Biennial PtConf 1999



Algorithm Analysis and Mapping Environment for Adaptive Computing Systems

Eric Pauer, Cory Myers, Ken Smith, and Paul Fiore

er.pauer, cory.mymr, ken.smith, paul.fiore@sanders.com

Lockheed Martin Company
Nashua, NH 03061



Third Bi-Annual Ptolemy Miniconference - 1999

ACS Domain - CGFPGA Target

Winograd dataflow (ACS domain)



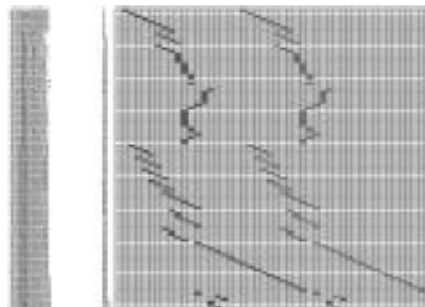
CGFPGA
target yields:
VHDL design
and schedule

VHDL design (generated)

```

-- Completion signals
Done <= '0';
Wait_AlgFin <= '1';
case Addr_State is
when Init_State =>
  if (Done <= '0') then
    Next_Adr_State <= Code1;
  else
    Next_Adr_State <= Init_State;
  end if;
when Code1 =>
  Next_Adr_State <= Code2;
  UC_Adrn_Control <= '1';
when Code2 =>
  Next_Adr_State <= Code3;
  --Address generator (adder) preloaded generator
  ADR_ILR <= '1';
when Code3 =>
  if (UC_Carry(9) <= '0') then
    Next_Adr_State <= Init_State;
    Done <= '1';
    Wait_AlgFin <= '0';
  else
    --Word counter control generator
    UC_ILR <= '1';
    --Address count enable engaged
    ADR_ILR <= '1';
    Next_Adr_State <= Code3;
  end if;
end case;
--End: Ptolemy2/ACS/ACS1.vhd

```



Dataflow/Hardware schedule

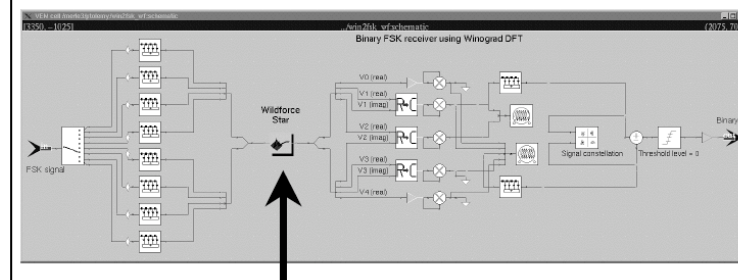
The results are sent to synthesis
and place/route, yielding
complete FPGA implementation!



Third Bi-Annual Ptolemy Miniconference - 1999

Hardware-in-the-loop

SDF Galaxy



SDF Wildforce star executes complete FPGA design
in hardware on Annapolis Wildforce FPGA board



Adaptive Computing System Design and Implementation using the ACS Domain

PUBS-98-MQ1_001-P
2/12/99 14



3rd Biennial PtConf 1999

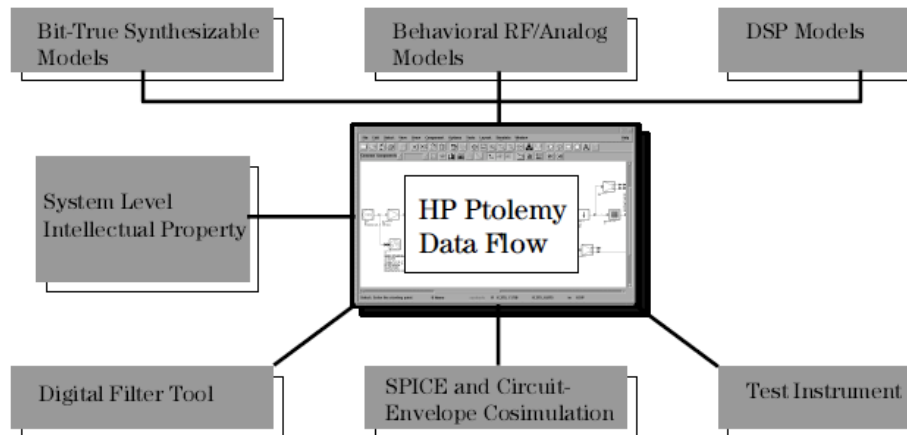


Cosimulating Synchronous DSP Designs with Analog RF Circuits

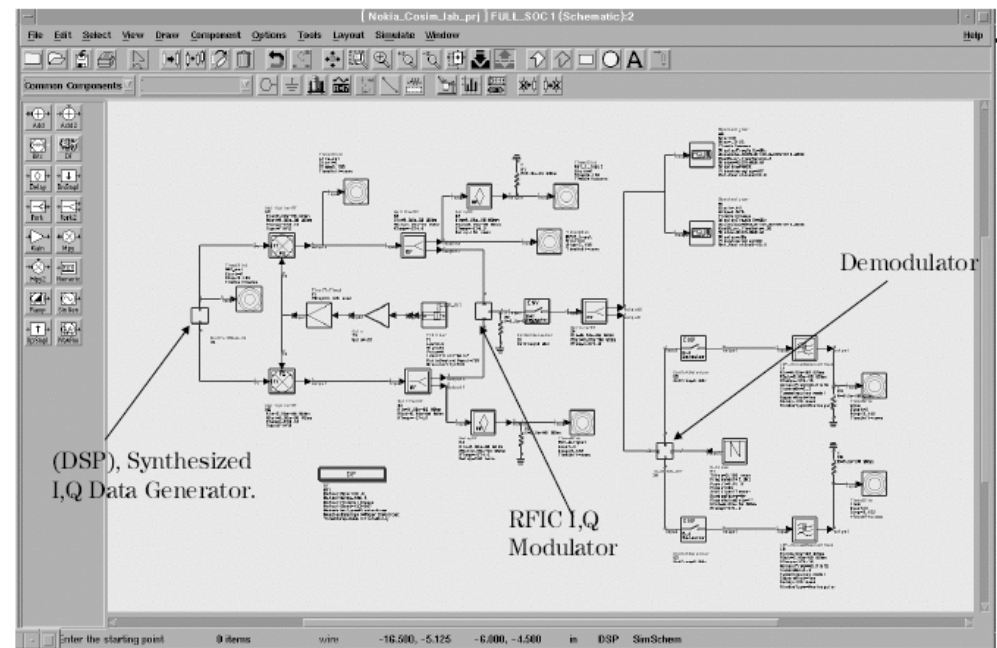
José Luis Pino and Khalil Kalbasi



HP Ptolemy



Example: 16 QAM Tx/Rx





4th

2001





4th 2001

Rapid Prototyping of RADAR Signal Processing Systems using Ptolemy Classic

Ptolemy MiniConference UCB

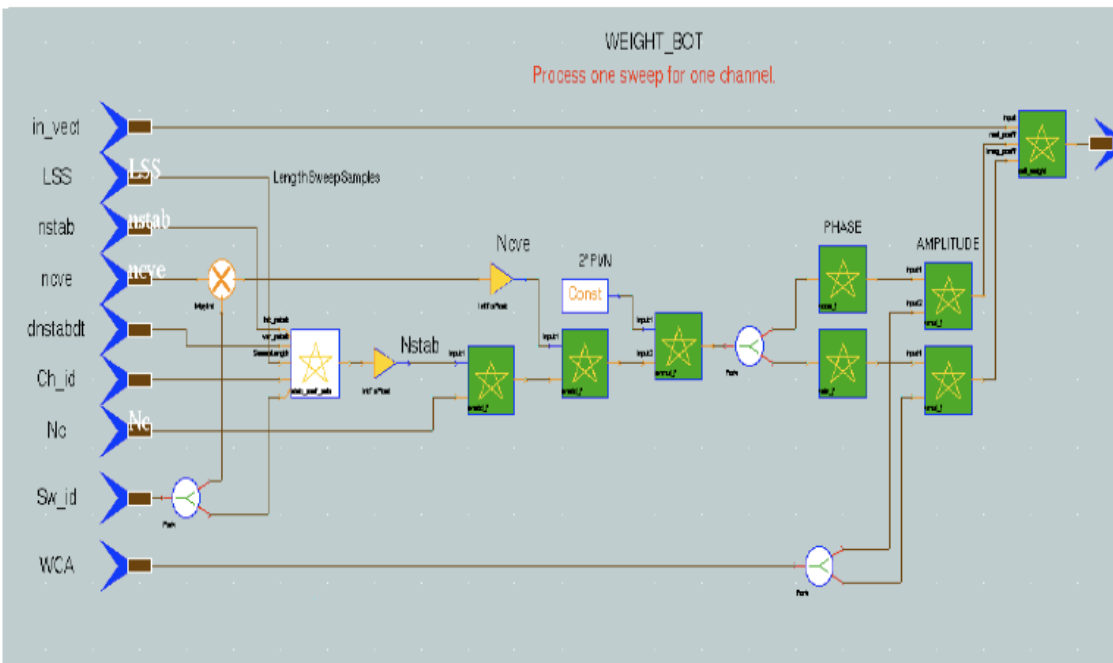
Denis Aulagnier, Patrick Meyer, Hans Schurer, Xavier Warzee,
THALES

THALES

Matra BAe Dynamics

BAE SYSTEMS

D. Aulagnier/P. Meyer/H. Schurer/X. Warzee, p1
THOMSON MARCONI
SONAR



CONCLUSIONS (1)

- Main functional requirements are met by the final design (12 of the 19 requirements)
- Throughput and latency requirements are almost met; expected to be met in case of full speed G4 daughter cards and/or VSIPL functions redesign
- Review of graphical Ptolemy designs seems faster and more efficient than code reviews
 - Disadvantage is parameter handling and scope.
 - Design is highly multi-rate, but this is difficult to see
 - Some functionality is inside stars (hidden)
- Total design, validate & test time for bare beamformer was 354.5 hours, while normal development takes 481 hours: **Approximately 36% faster (improvement ~1.36)**

5th 2003

CHI

Director:

- Edward A. Lee

Staff:

- Christopher Hylands
- Susan Gardner (Chess)
- Nuala Mansard
- Mary P. Stewart
- Neil E. Turner (Chess)
- Lea Turpin (Chess)

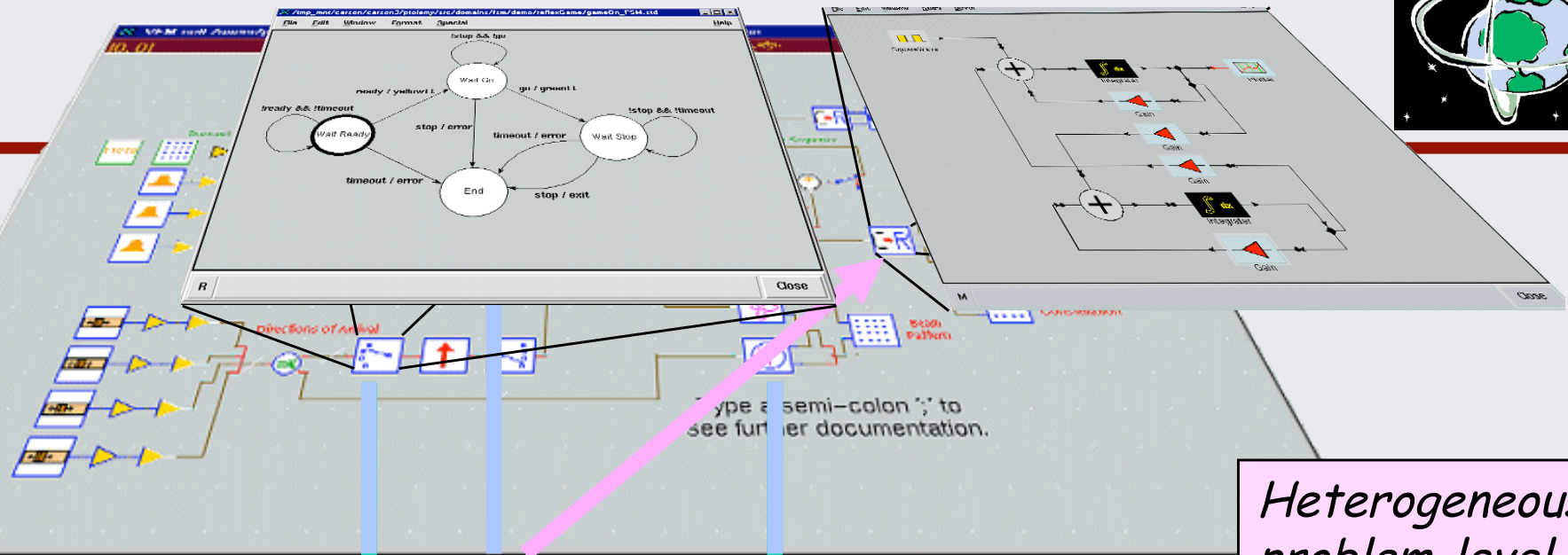
Postdocs, Etc.:

- Joern Janneck, Postdoc
- Rowland R. Johnson, Visiting Scholar
- Kees Vissers, Visiting Industrial Fellow
- Daniel Lázaro Cuadrado, Visiting Scholar

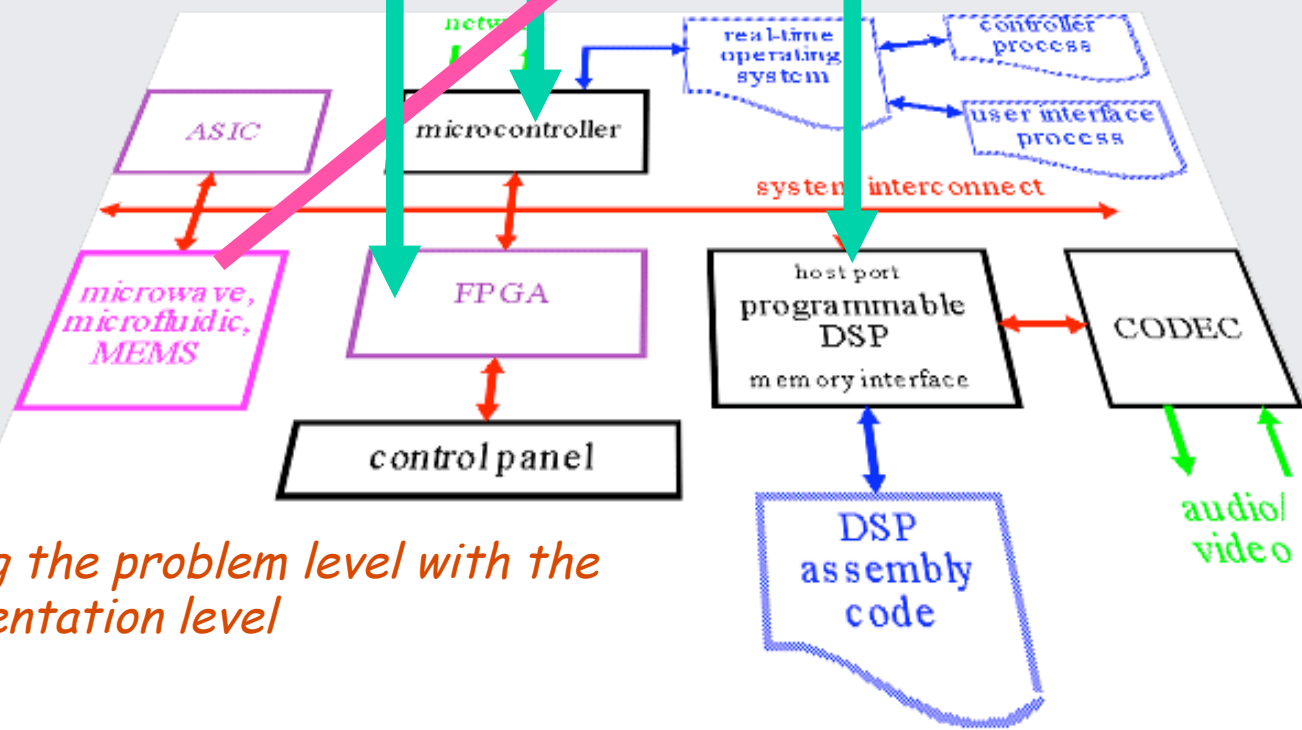
Graduate Students:

- J. Adam Cataldo
- Chris Chang
- Elaine Cheong
- Sanjeev Kohli
- Xiaojun Liu
- Eleftherios D. Matsikoudis
- Stephen Neuendorffer
- James Yeh
- Yang Zhao
- Haiyang Zheng
- Rachel Zhou





*Heterogeneous,
problem-level
description*



*Heterogeneous,
implementation-
level description*

*Relating the problem level with the
implementation level*

Foundations



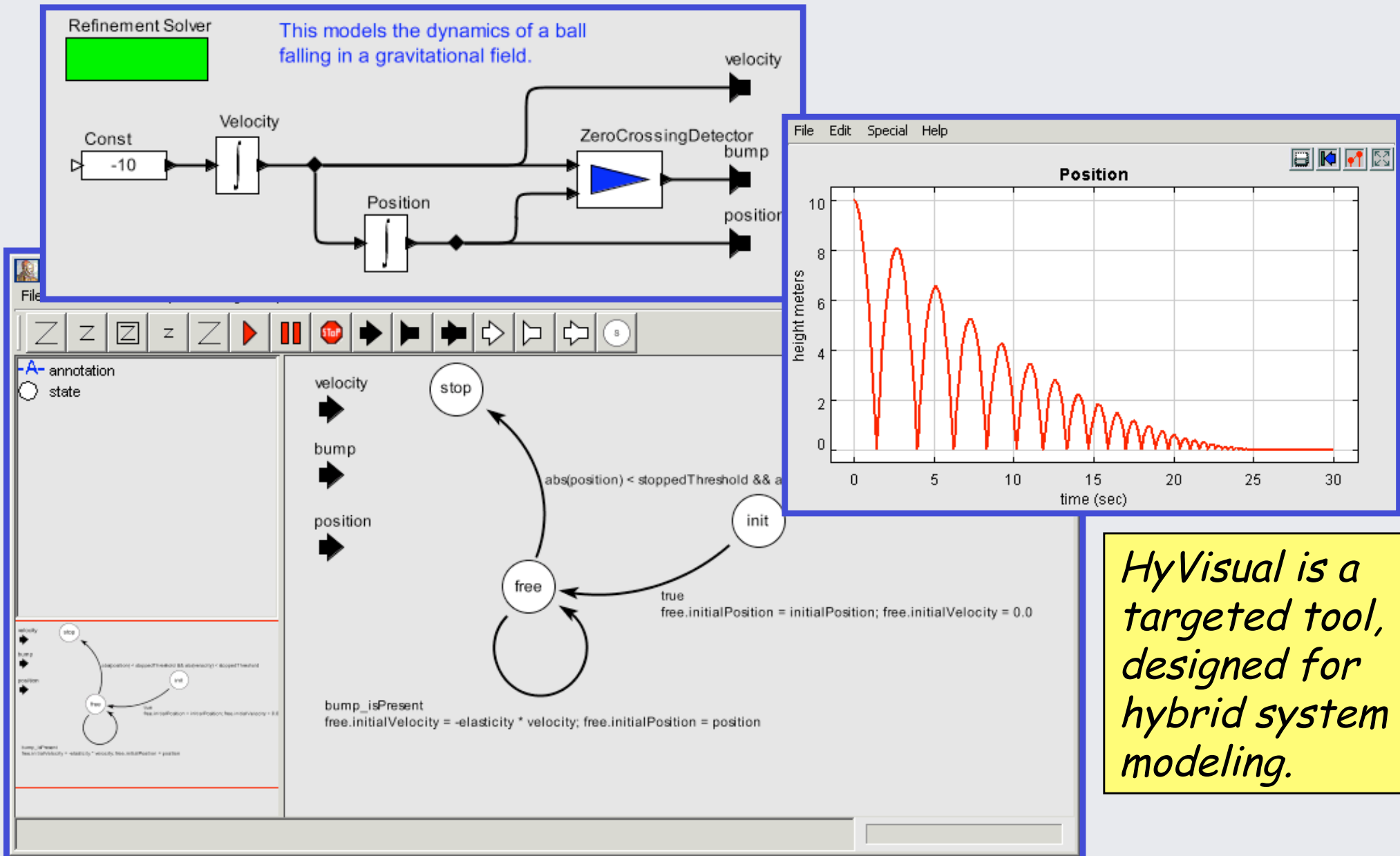
Our contributions:

- Behavioral Types
- Domain Polymorphism
- Responsible Frameworks
- Hybrid Systems Semantics
- Dataflow Semantics
- Tagged Signal Model
- Starcharts and Modal Model Semantics
- Discrete-Event Semantics
- Continuous-Time Semantics

Giving structure to the notion of
"models of computation"



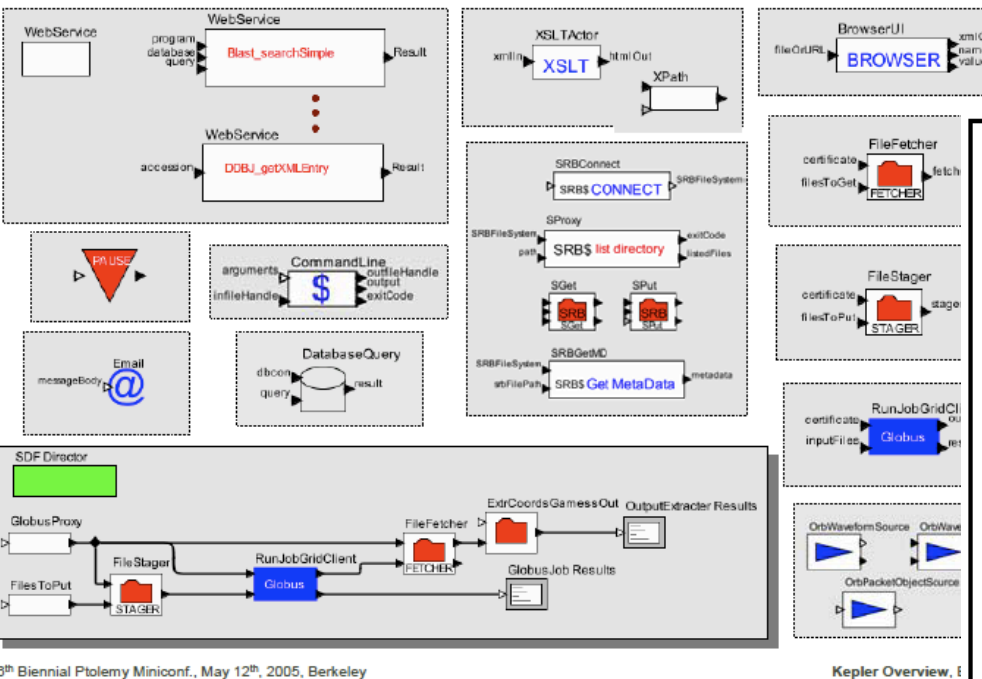
HyVisual - Hybrid System Modeling Tool Based on Ptolemy II, Released Jan. 2003





6th 2005

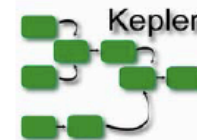
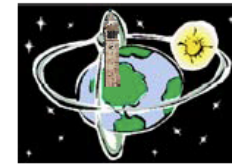
Some KEPLER Actors (out of 160+ ... and counting...)



6th Biennial Ptolemy Miniconf., May 12th, 2005, Berkeley

Kepler Overview, I

KEPLER: Overview and Project Status



Bertram Ludäscher
ludaesch@ucdavis.edu

Associate Professor
Dept. of Computer Science & Genome Center
University of California, Davis



KEPLER/CSP: Contributors, Sponsors, Projects

Ilkay Altintas *SDM, NLADR, Resurgence, EOL, ...*
Kim Baldridge *Resurgence, NMI*
Chad Berkley *SEEK*
Shawn Bowers *SEEK*
Terence Critchlow *SDM*
Tobin Fricke *ROADNet*
Jeffrey Grethe *BIRN*
Christopher H. Brooks *Ptolemy II*
Zhengang Cheng *SDM*
Dan Higgins *SEEK*
Efrat Jaeger *GEON*
Matt Jones *SEEK*
Werner Krebs, *EOL*
Edward A. Lee *Ptolemy II*
Kai Lin *GEON*

www.kepler-project.org

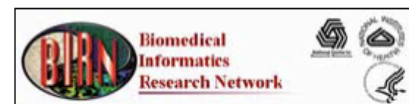
LLNL, NCSU, SDSC, UCB, UCD, UCSB,
UCSD, U Man... Utah, ..., UTEP, ..., Zurich

Bertram Ludäscher *SDM, SEEK, GEON, BIRN, ROADNet*
Mark Miller *EOL*
Steve Mock *NMI*
Steve Neuendorffer *Ptolemy II*
Jing Tao *SEEK*
Mladen Vouk *SDM*
Xiaowen Xin *SDM*
Yang Zhao *Ptolemy II*
Bing Zhu *SEEK*
...

Collab. tools: IRC, cvs, skype, Wiki: hotTopics, FAQs, ..



Ptolemy II



Kepler Overview, B. Ludäscher

Ptolemy Project, Berkeley 22



6th 2005

Growth of the Cal actor language

driver application

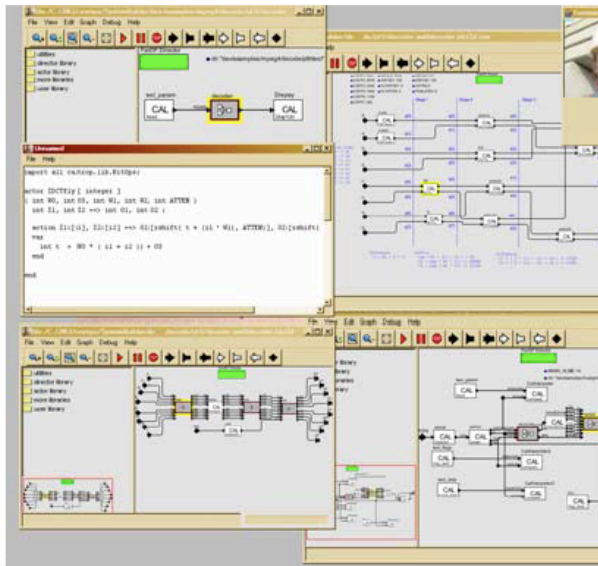
MPEG-4 decoder

metrics

- 60 atomic actors
- 22 atomic actor classes
- 3307 LOC (Cal)
- LOC per actor class between 7 and 2054

actor constructs

- variable token rates
- static/cyclostatic rates
- data-dependent choice
- test for absence of tokens
 - non-prefix-monotonic actors



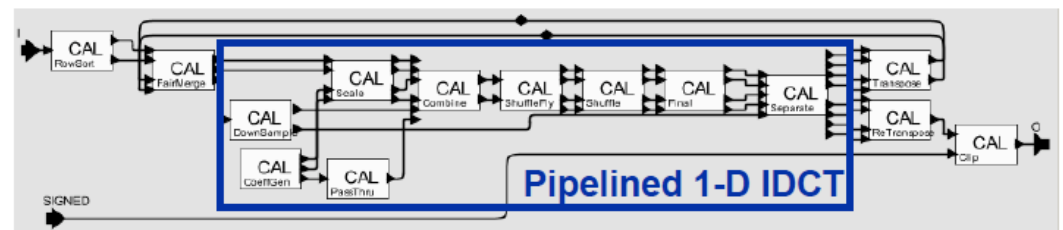
Programming with actors

Jörn W. Janneck
Xilinx Research Labs

code generation

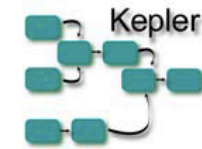
2D-IDCT, version 2

- interleave row and column streams
- pipelined 1D-IDCT
- result:
 - 6 multipliers with 46% utilization
 - more operator re-use costly in terms of operand routing
 - >100 Mhz clock





7th 2007



The Kepler Project

Overview, Status, and Future Directions

Matthew B. Jones
on behalf of the Kepler Project team

National Center for Ecological Analysis and Synthesis
University of California, Santa Barbara



REAP breakdown

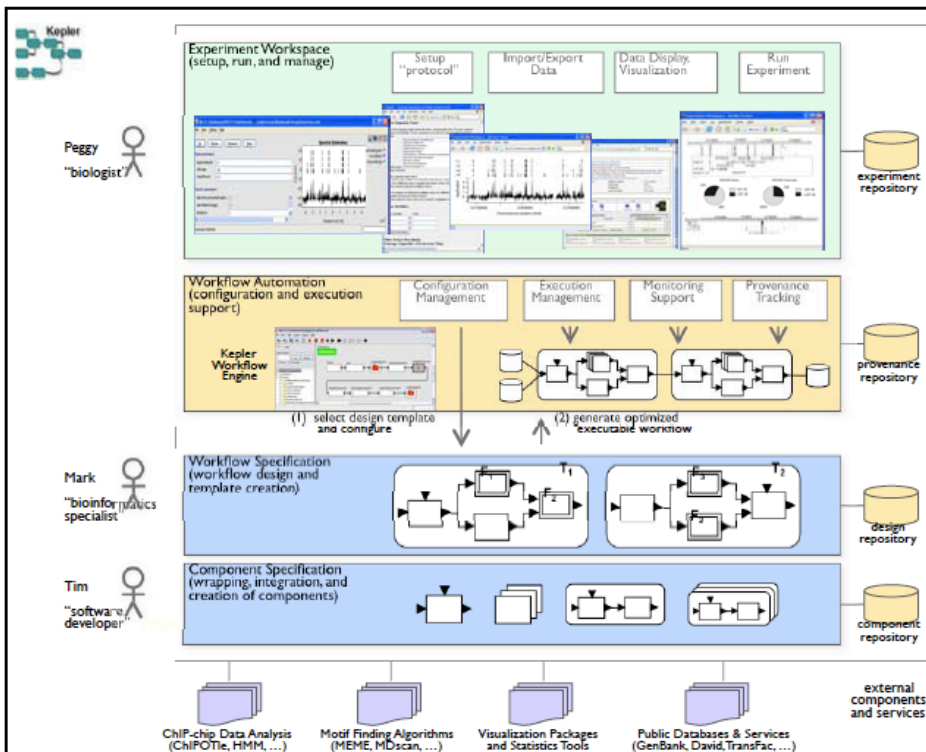
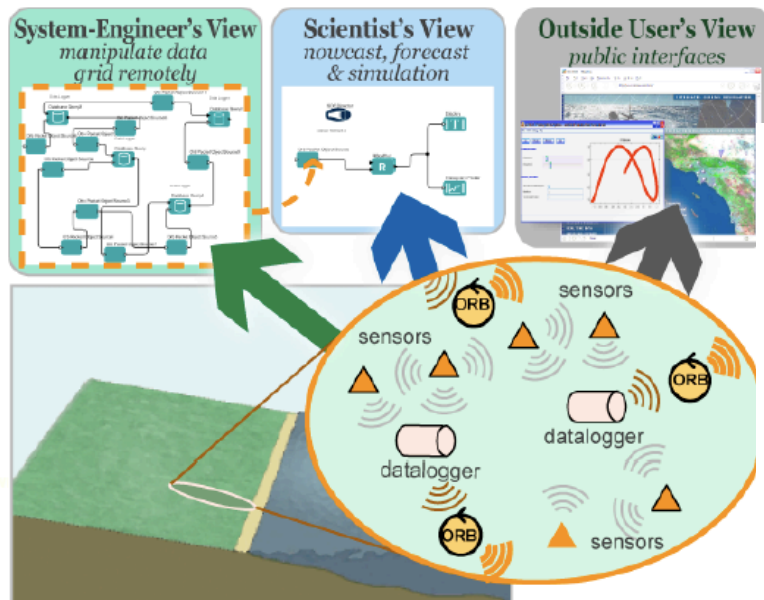


Figure from Bowers and McPhillips



8th 2009

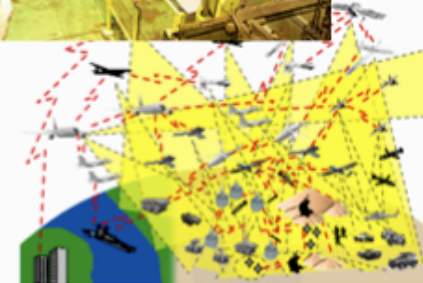
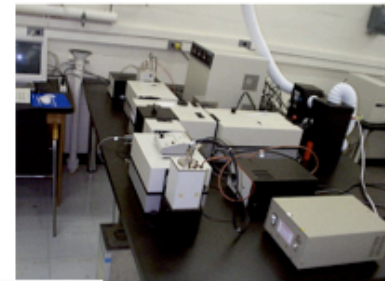
Hugo Andrade (NI)
 Christopher Brooks
 Dai Bui
 Yasemin Demir
 John Eidson (Agilent)
 Thomas Feng
 Shanna Shaye Forbes
 Jeff Jensen
 Edward Lee
 Jackie Leung
 Ben Lickly
 Isaac Liu
 Thomas Mandl (Bosch)
 Slobodan Matic
 Eleftherios Matsikoudis
 Hiren Patel
 Stephan Resmerita
 Bert Rodiers
 Yang Zhao
 Jia Zou



Cyber-Physical Systems (CPS)

Where it is going

CPS: Orchestrating networked computational resources with physical systems.





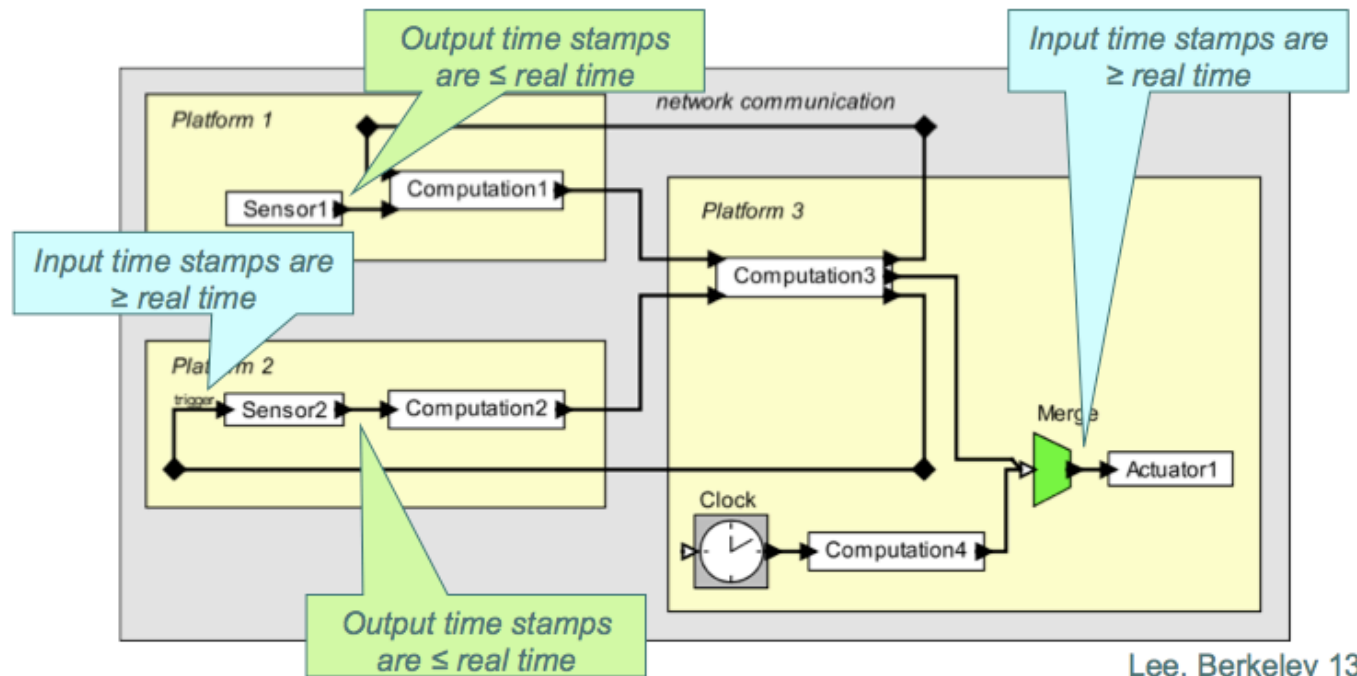
8th 2009

Hugo Andrade (NI)
Christopher Brooks
Dai Bui
Yasemin Demir
John Eidson (Agilent)
Thomas Feng
Shanna Shaye Forbes
Jeff Jensen
Edward Lee
Jackie Leung
Ben Lickly
Isaac Liu
Thomas Mandl (Bosch)
Slobodan Matic
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Stephan Resmerita
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Jia Zou



PTIDES: Programming Temporally Integrated Distributed Embedded Systems

Distributed execution under DE semantics, with “model time” and “real time” bound at sensors and actuators.



Lee, Berkeley 13

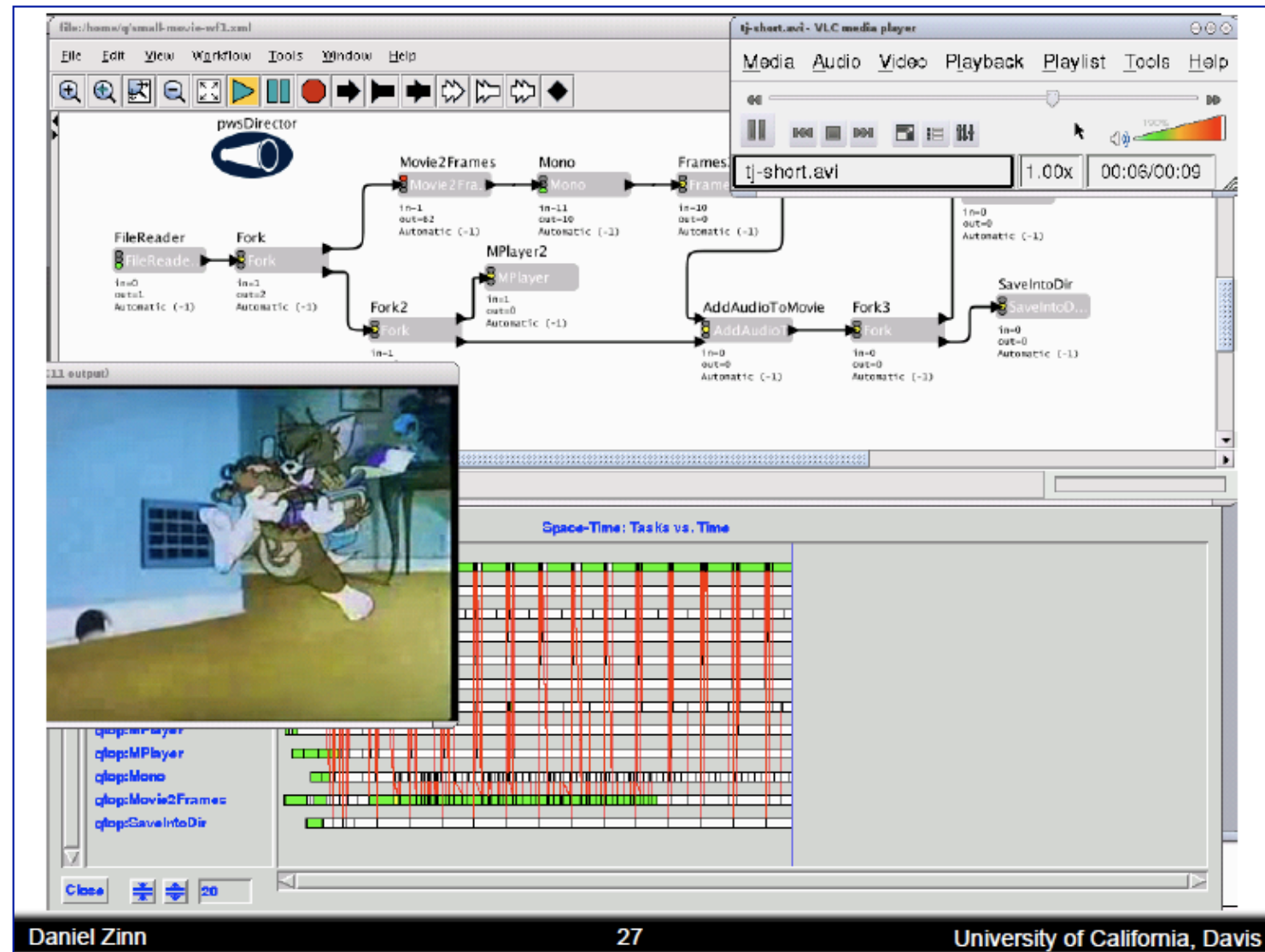


8th 2009

Parallel Virtual Machines in Kepler

Daniel Zinn
Xuan Li
Bertram Ludaescher

UC Davis





9th 2011

Let the show begin!