CHESS
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The Distributed Power System Test Case for Distributed Real-Time Systems

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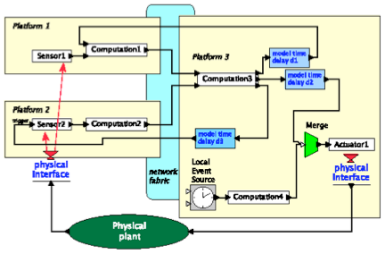
Hardware for this research is provided by National Instruments and Renesas

Distributed Real-Time System Implementation

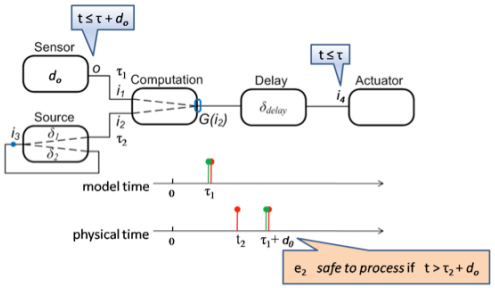


Programming Model

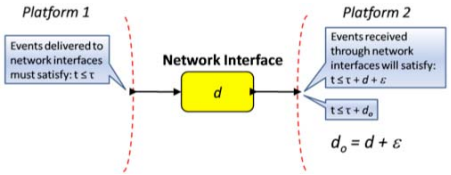
Programming **T**emporally **I**ntegrated **D**istributed **E**mbedded **S**ystems

Based on Discrete-Event semantics Event processing in time-stamp order

Relates *model time* to *physical time* at environment interfaces
d_o – sensor latency

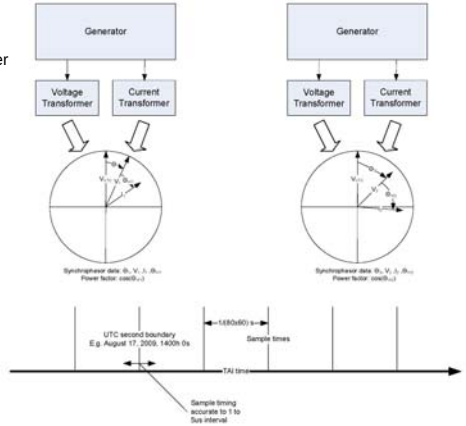


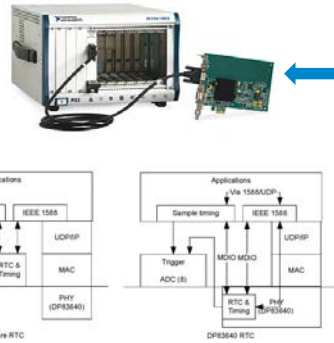
Leverages time synchronization across distributed platforms
(IEEE 1588 protocol over Ethernet)
d – comm. latency, ε – sync. error



Distributed Testbed Objectives

- Safe event processing
  Bounded latency between hardware components
  Distribution: bounded-delay networking protocol
- Expressiveness of interaction
  Complexity of real sensor, actuator and network interfaces
- Timing support
  External to microprocessor
  National Semiconductor DP83640: IEEE 1588 enabled PHY chip
- Scheduling
  Deadlines defined by sensor – actuator model delays
  Distribution: local from end-to-end deadlines
- Network addressing
- Visibility during model-based design





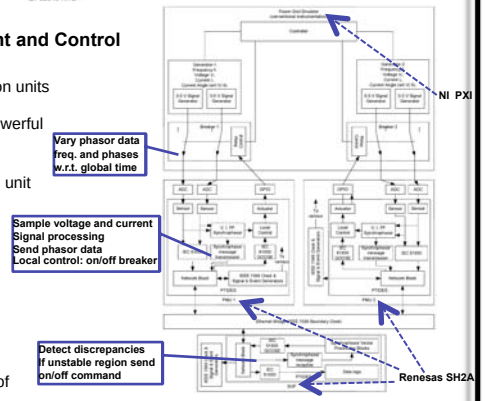
DP83640: PHY chip with PTP

Clock (read/write/adjust/scale)
TX Pkt Parser and TS unit
RX Pkt Parser and TS Unit
8 Triggers
8 Event TS
6 GPIOs4

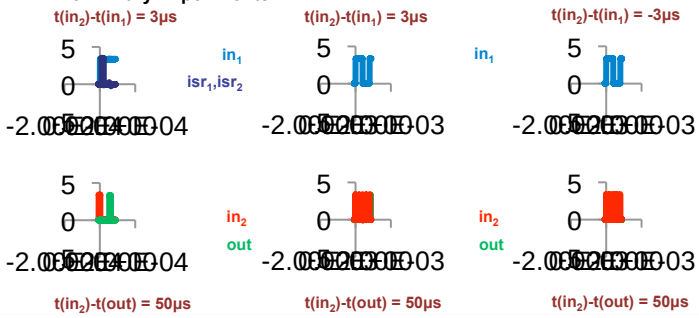
Synchrophasor-based Measurement and Control

- Frequency and phase of power generation units must remain synchronous
- Synchrophasor technology provides a powerful tool to directly measure the state
- PMU = Primary Measurement Unit
  SVP = Synchrophasor Vector Processing unit

Real PTIDES problem
- Tight (1-5us) timing accuracy
- Reasonable sample rate (4.8 KSPS)
- Timing based on UTC
- Multiple functions run concurrently (UDP, PTP)
- Naturally distributed due to physical size of grid



Preliminary Experiments



Ptolemy Approximation Model