Berkeley Verification and Synthesis Research Center

ABC - a tool for sequential logic verification and synthesis

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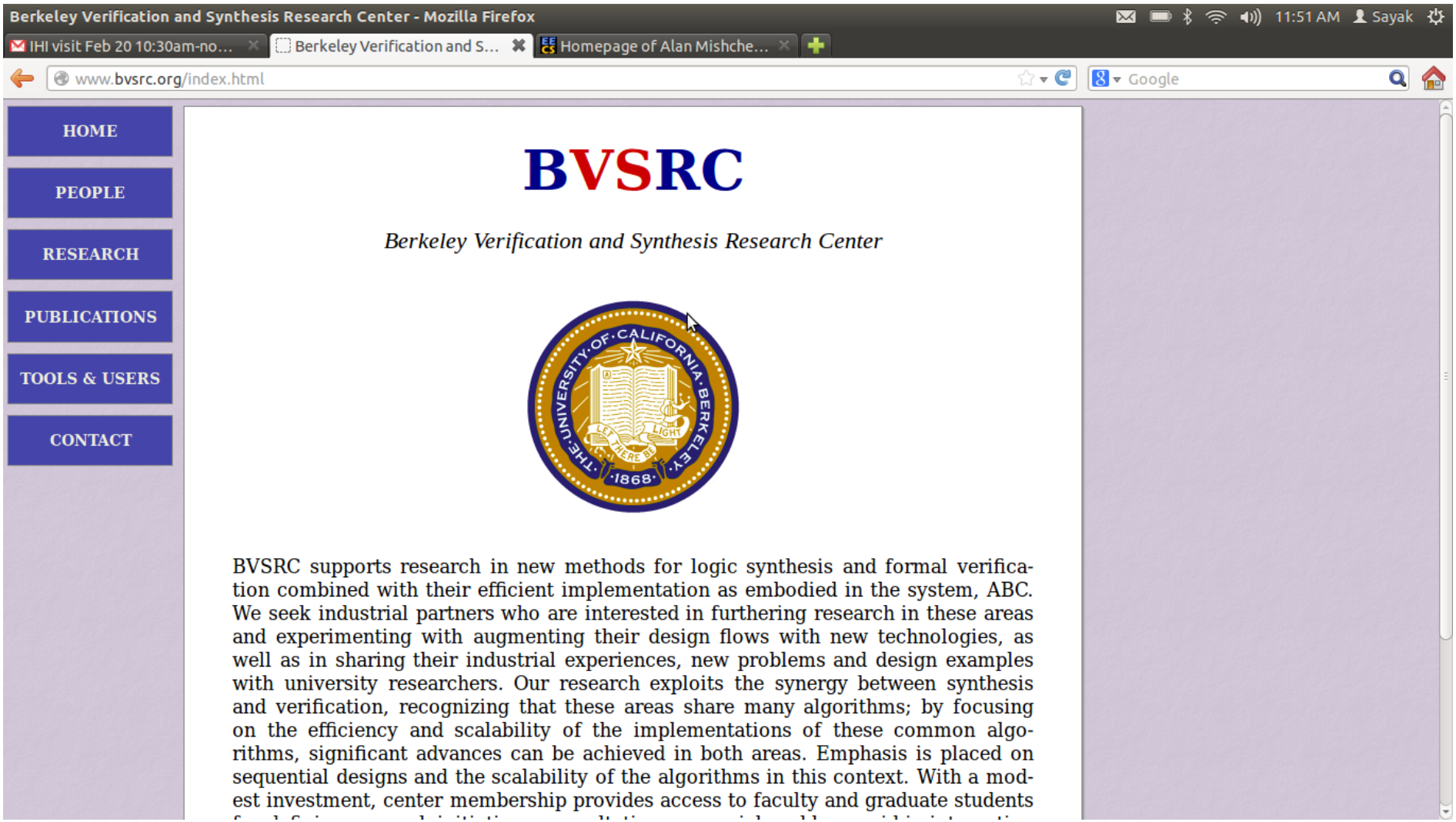
University of California, Berkeley

Our Research Group



Our Research Group - People

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Staff



Robert Brayton
(Prof. and Director)

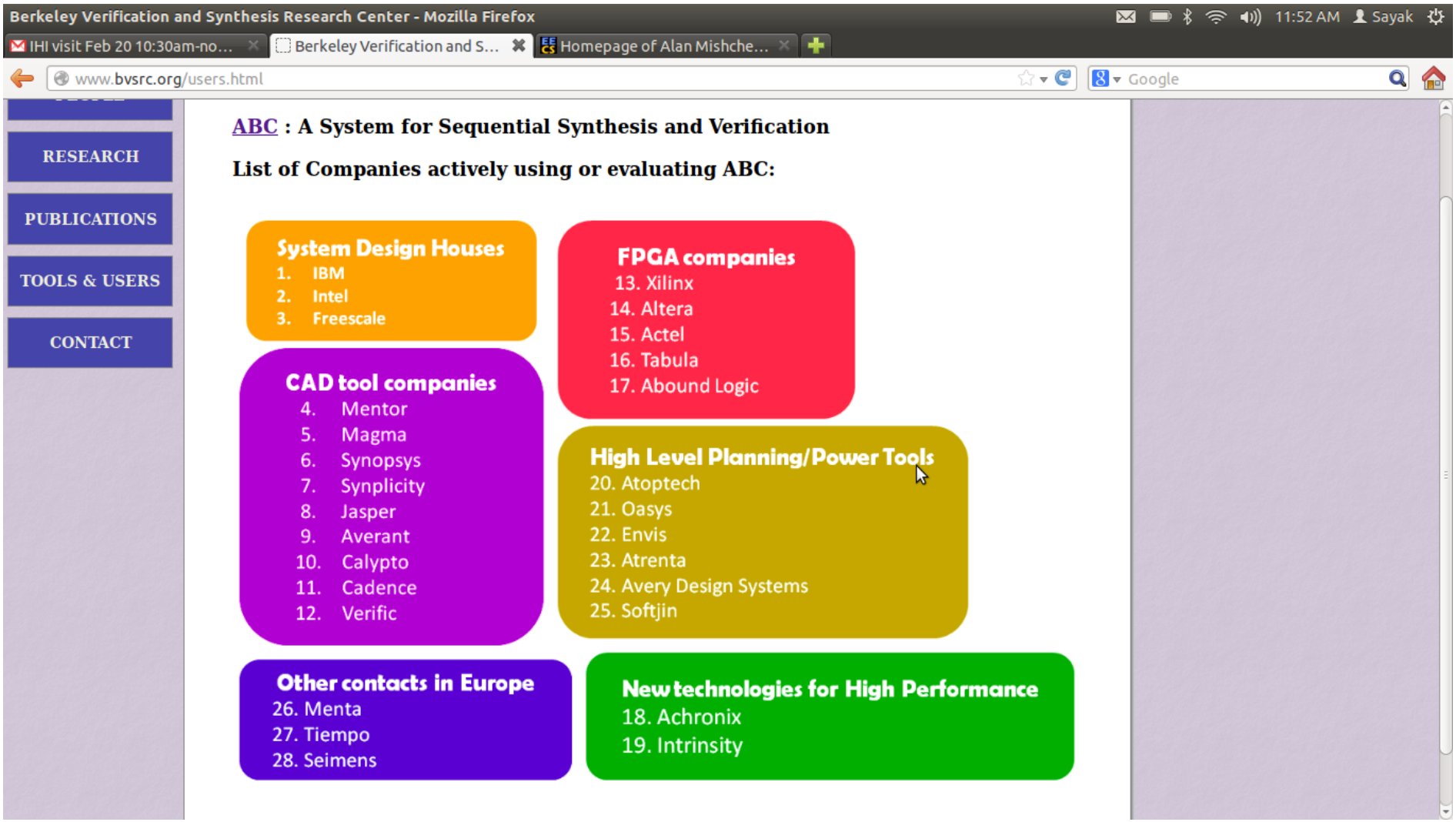
Alan Mishchenko
(Research Engineer)

Niklas Een
(Research Engineer)

Graduate Students

- Sayak Ray
- Baruch Sterin
- Jiang Long
- Zile Wei

Users of ABC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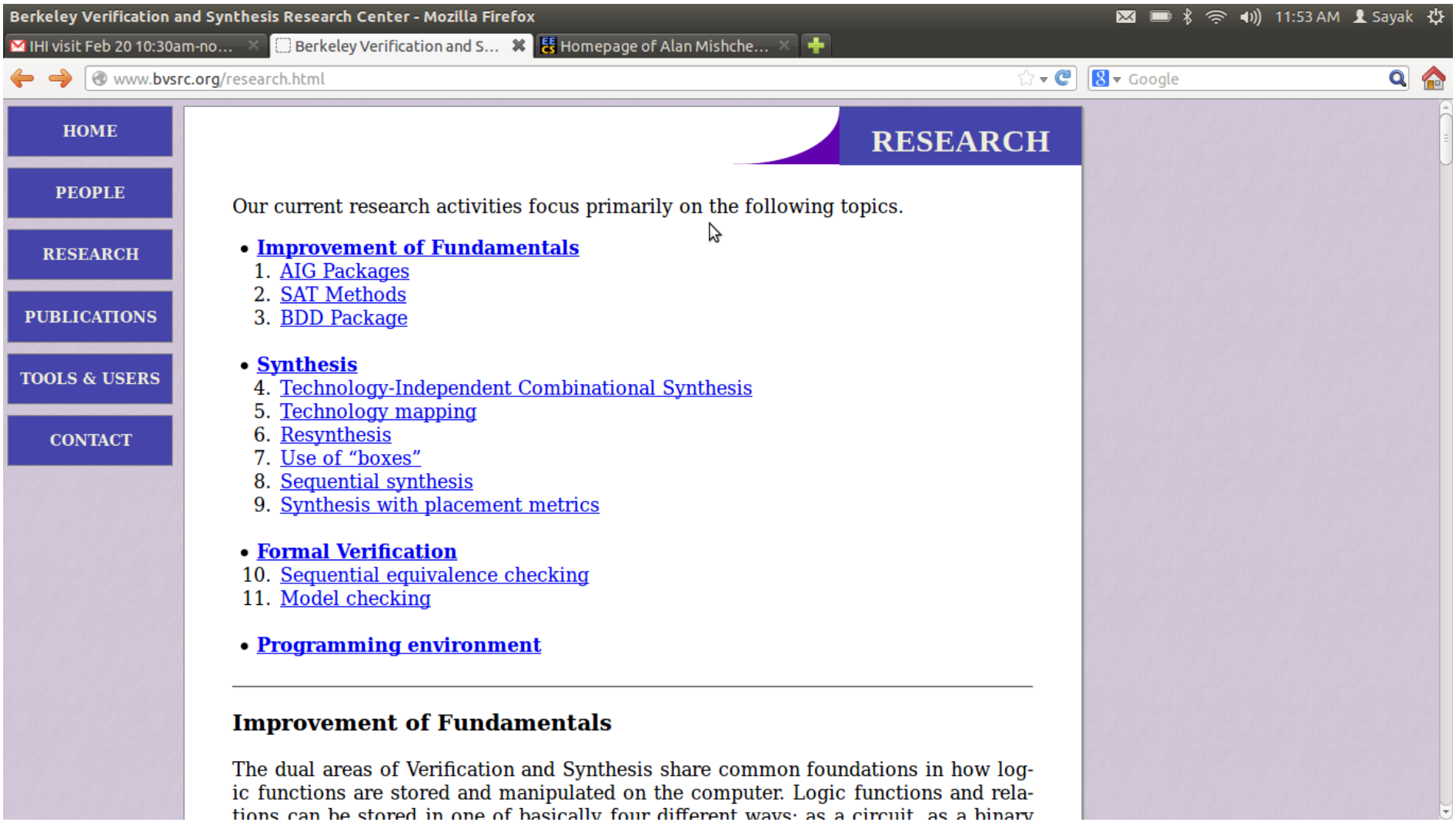
ABC : A System for Sequential Synthesis and Verification
List of Companies actively using or evaluating ABC:
System Design Houses
1. IBM
2. Intel
3. Freescale
FPGA companies
13. Xilinx
14. Altera
15. Actel
16. Tabula
17. Abound Logic
CAD tool companies
4. Mentor
5. Magma
6. Synopsys
7. Synplicity
8. Jasper
9. Averant
10. Calypto
11. Cadence
12. Verific
High Level Planning/Power Tools
20. Atoptech
21. Oasys
22. Envis
23. Atrenta
24. Avery Design Systems
25. Softjin
Other contacts in Europe
26. Menta
27. Tiempo
28. Seimens
New technologies for High Performance
18. Achronix
19. Intrinsity

BVSRC Research



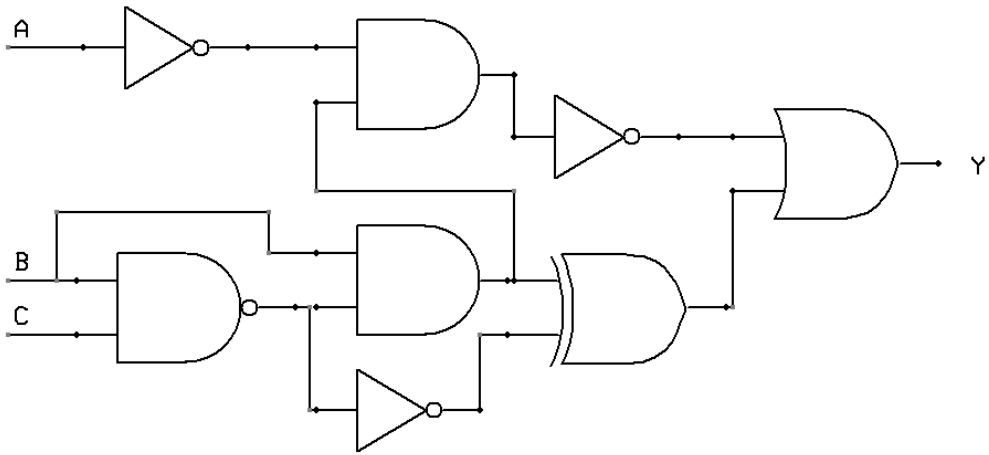
Scope Of ABC

- Combinational and Sequential Logic Optimization
- Combinational and Sequential Equivalence Checking
- Property Verification (Model Checking)
- **Winner of 2012, 2011, 2010 Hardware Model Checking Contest**

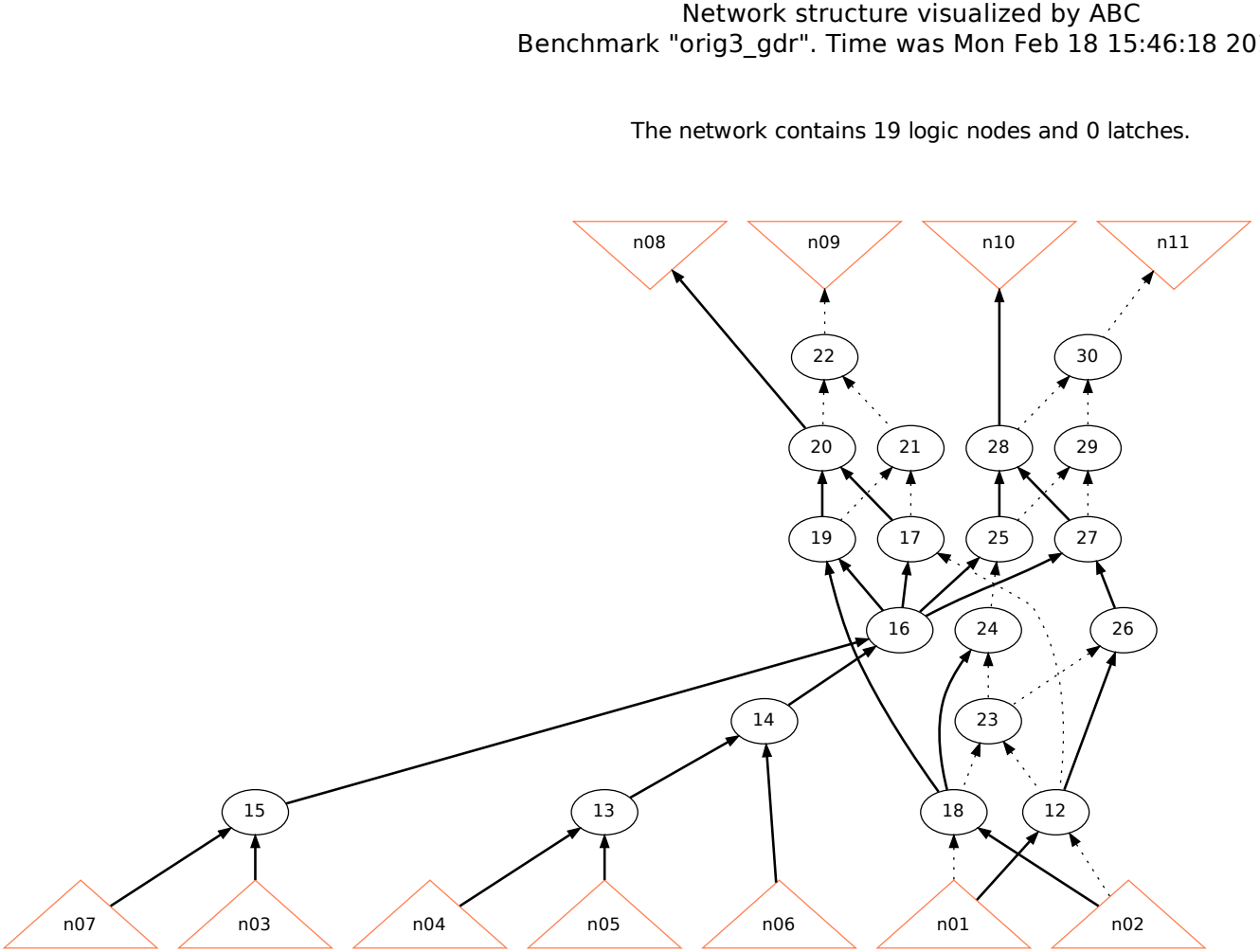
Working With ABC

- A command-line tool
- Synthesis and analysis framework for digital logic circuits
- Input format - BLIF, AIG

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



AIG - the data structure for ABC



Sequential Circuits

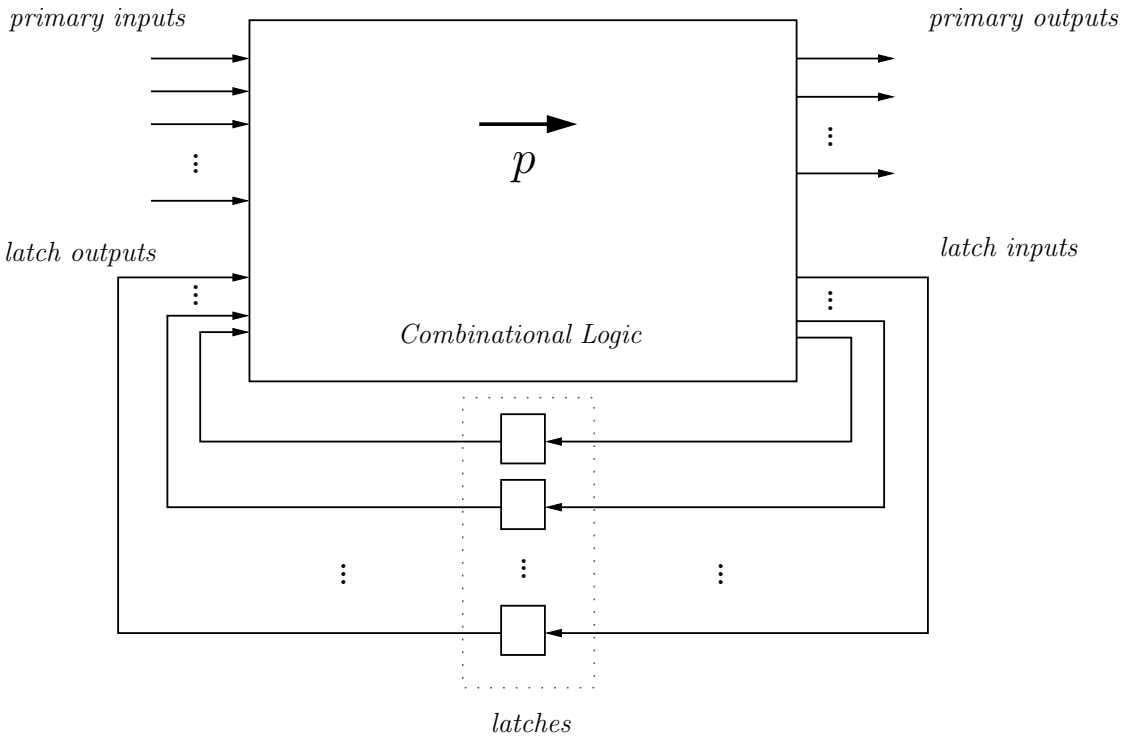


Figure: A Sequential Circuit

Sequential Circuits - Model Checking

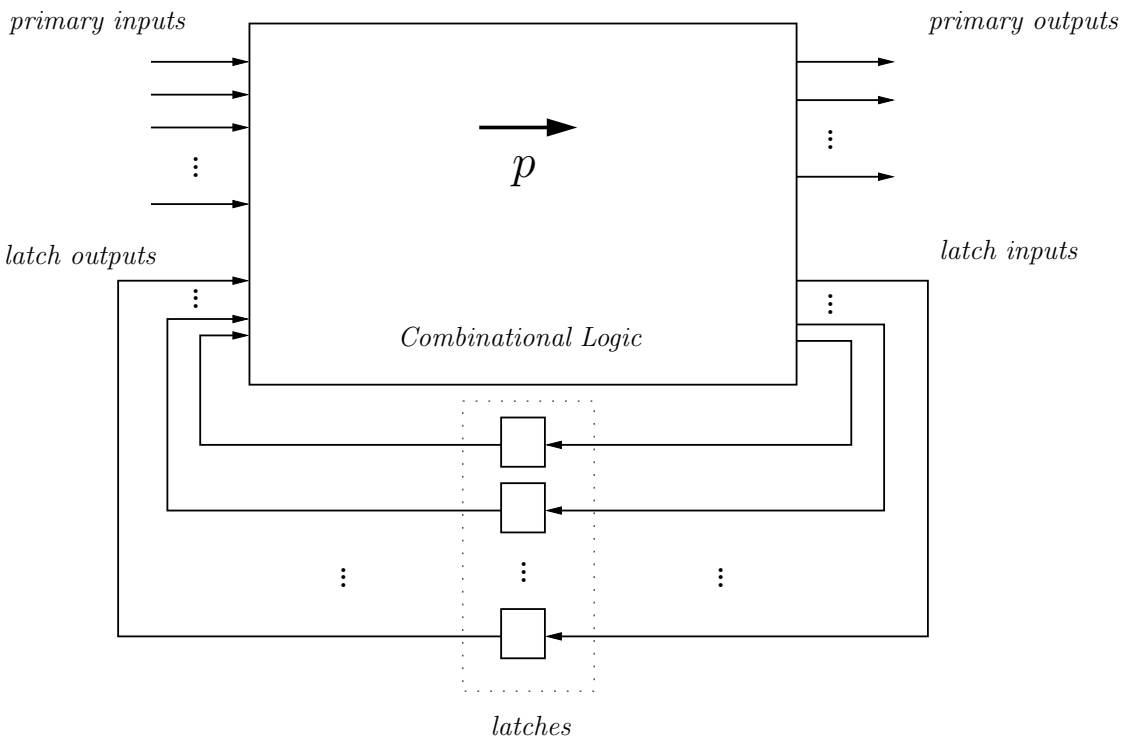


Figure: A Sequential Circuit