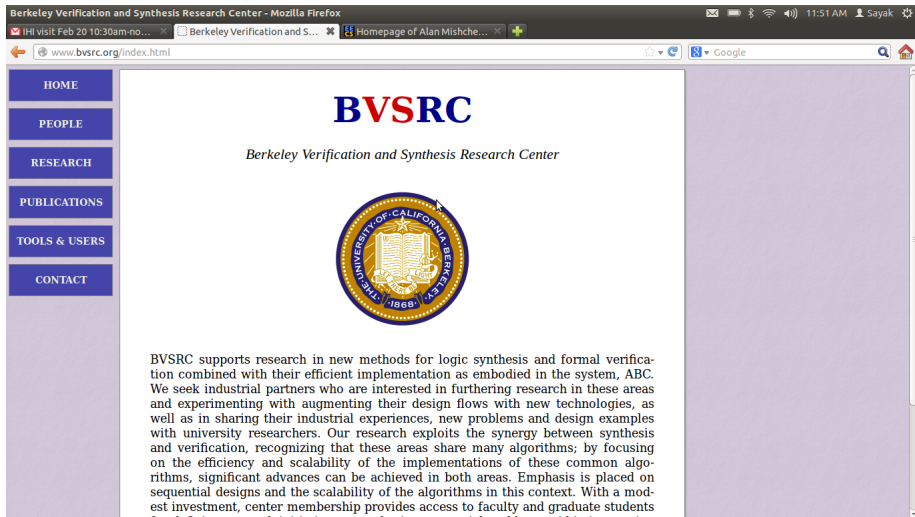


# Berkeley Verification and Synthesis Research Center

## ABC - a tool for sequential logic verification and synthesis

Sayak Ray  
{sayak@eecs.berkeley.edu}  
University of California, Berkeley

# Our Research Group




The screenshot shows a Mozilla Firefox browser window displaying the homepage of the Berkeley Verification and Synthesis Research Center (BVSRC). The browser's address bar shows the URL `www.bvsrc.org/index.html`. The page features a navigation menu on the left with links for HOME, PEOPLE, RESEARCH, PUBLICATIONS, TOOLS & USERS, and CONTACT. The main content area displays the BVSRC logo, which consists of the letters "BVSRC" in a stylized font, followed by the text "Berkeley Verification and Synthesis Research Center" and the official seal of the University of California, Berkeley. Below the logo, a paragraph of text describes the center's research focus on logic synthesis and formal verification.

Berkeley Verification and Synthesis Research Center - Mozilla Firefox

www.bvsrc.org/index.html

**BVSRC**

*Berkeley Verification and Synthesis Research Center*



BVSRC supports research in new methods for logic synthesis and formal verification combined with their efficient implementation as embodied in the system, ABC. We seek industrial partners who are interested in furthering research in these areas and experimenting with augmenting their design flows with new technologies, as well as in sharing their industrial experiences, new problems and design examples with university researchers. Our research exploits the synergy between synthesis and verification, recognizing that these areas share many algorithms; by focusing on the efficiency and scalability of the implementations of these common algorithms, significant advances can be achieved in both areas. Emphasis is placed on sequential designs and the scalability of the algorithms in this context. With a modest investment, center membership provides access to faculty and graduate students

# Our Research Group - People

Berkeley Verification and Synthesis Research Center - Mozilla Firefox

IHI visit Feb 20 10:30am-no... x Berkeley Verification and S... x Homepage of Alan Mishche... x

www.bvsrc.org/people.html

HOME

PEOPLE

RESEARCH


PUBLICATIONS

TOOLS & USERS


CONTACT

## PEOPLE


### Staff



**Robert Brayton**  
(Prof. and Director)



**Alan Mishchenko**  
(Research Engineer)



**Niklas Een**  
(Research Engineer)

### Graduate Students

- Sayak Ray
- Baruch Sterin
- Jiang Long
- Zile Wei

# Users of ABC

Berkeley Verification and Synthesis Research Center - Mozilla Firefox

www.bvsrc.org/users.html

## ABC : A System for Sequential Synthesis and Verification

### List of Companies actively using or evaluating ABC:

- System Design Houses**
  1. IBM
  2. Intel
  3. Freescale
- FPGA companies**
  13. Xilinx
  14. Altera
  15. Actel
  16. Tabula
  17. Abound Logic
- CAD tool companies**
  4. Mentor
  5. Magma
  6. Synopsys
  7. Synplicity
  8. Jasper
  9. Averant
  10. Calypto
  11. Cadence
  12. Verific
- High Level Planning/Power Tools**
  20. Atoptech
  21. Oasys
  22. Envis
  23. Atrenta
  24. Avery Design Systems
  25. Softjin
- Other contacts in Europe**
  26. Menta
  27. Tiempo
  28. Seimens
- New technologies for High Performance**
  18. Achronix
  19. Intrinsicity

Berkeley Verification and Synthesis Research Center - Mozilla Firefox

www.bvsrc.org/research.html

RESEARCH

Our current research activities focus primarily on the following topics.

- **Improvement of Fundamentals**
  1. [AIG Packages](#)
  2. [SAT Methods](#)
  3. [BDD Package](#)
- **Synthesis**
  4. [Technology-Independent Combinational Synthesis](#)
  5. [Technology mapping](#)
  6. [Resynthesis](#)
  7. [Use of "boxes"](#)
  8. [Sequential synthesis](#)
  9. [Synthesis with placement metrics](#)
- **Formal Verification**
  10. [Sequential equivalence checking](#)
  11. [Model checking](#)
- **Programming environment**

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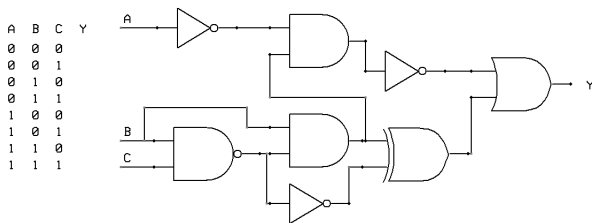
### Improvement of Fundamentals

The dual areas of Verification and Synthesis share common foundations in how logic functions are stored and manipulated on the computer. Logic functions and relations can be stored in one of basically four different ways: as a circuit, as a binary

- Combinational and Sequential Logic Optimization
- Combinational and Sequential Equivalence Checking
- Property Verification (Model Checking)
- **Winner of 2012, 2011, 2010 Hardware Model Checking Contest**

# Working With ABC

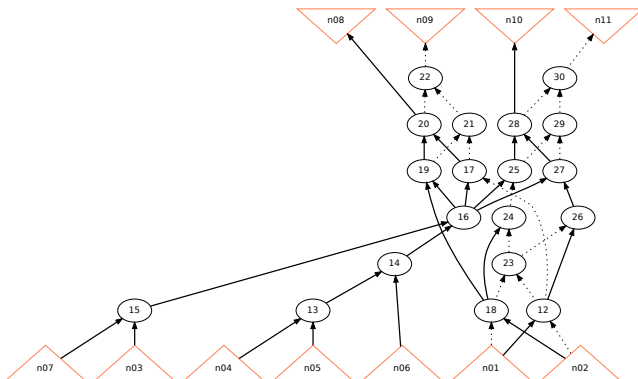
- A command-line tool
- Synthesis and analysis framework for digital logic circuits
- Input format - BLIF, AIG



# AIG - the data structure for ABC

Network structure visualized by ABC  
Benchmark "orig3\_gdr". Time was Mon Feb 18 15:46:18 2013.

The network contains 19 logic nodes and 0 latches.





# Sequential Circuits

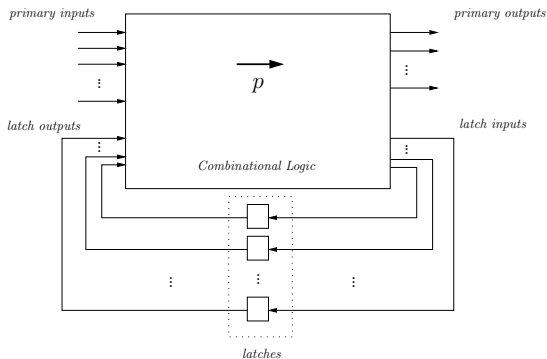


Figure: A Sequential Circuit

# Sequential Circuits - Model Checking

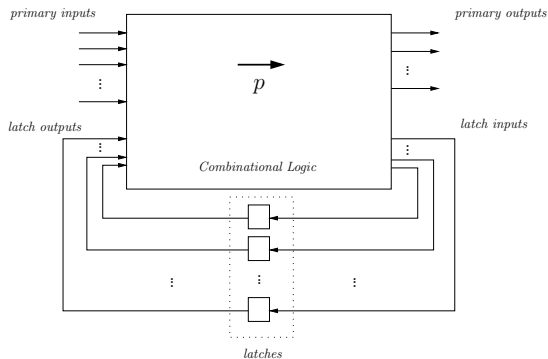


Figure: A Sequential Circuit

