CHESS
CENTER FOR HYBRID & EMBEDDED SOFTWARE SYSTEMS

Precision Timed Infrastructure

http://chess.eecs.berkeley.edu/

Organization

Staff

David Broman, UC Berkeley and Linköping University
Edward A. Lee, UC Berkeley
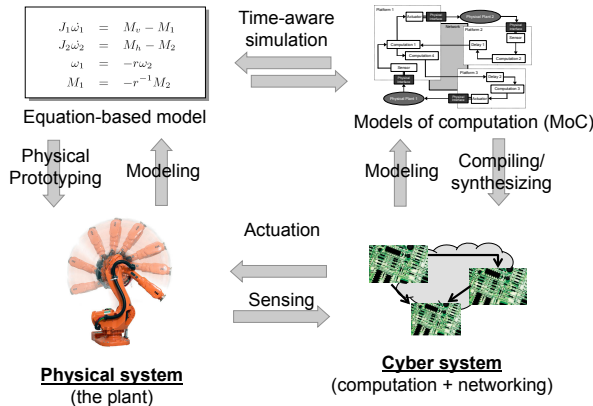Aviral Shrivastava, Arizona State University

Students

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Collaborators

Steven A. Edwards, Columbia University
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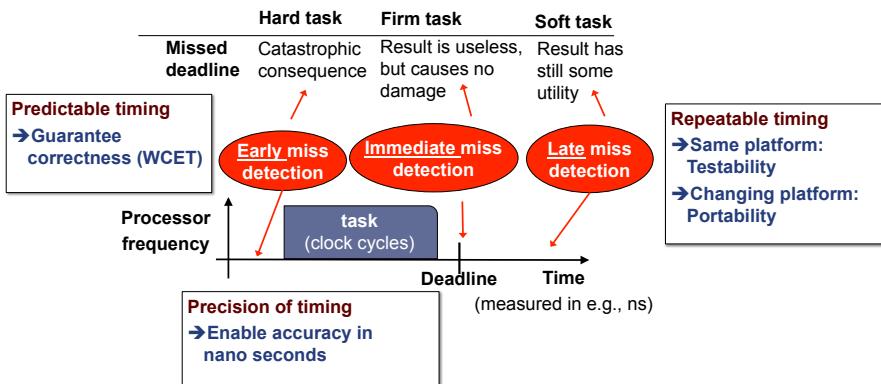Martin Schoeberl, Technical University of Denmark

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Cyber-Physical Systems

$$J_1\dot{\omega}_1 = M_v - M_1$$
$$J_2\dot{\omega}_2 = M_h - M_2$$
$$\omega_1 = -r\omega_2$$
$$M_1 = -r^{-1}M_2$$

Equation-based model

Time-aware simulation

Models of computation (MoC)

Physical Prototyping → Modeling

Modeling ← Compiling/ synthesizing

Actuation

Sensing

Physical system (the plant)
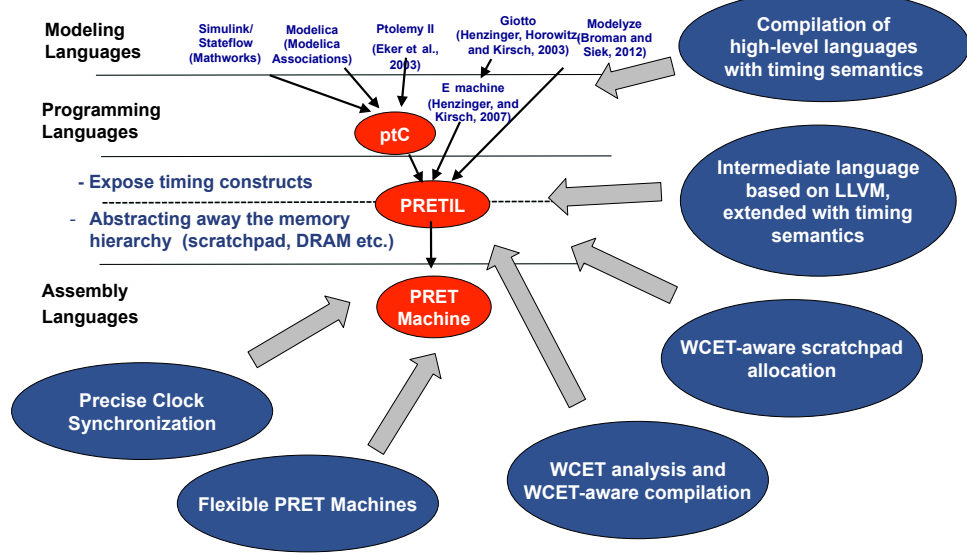
Cyber system (computation + networking)

Model fidelity problem

"Ensuring that the model accurately imitates the real system"

Overall challenge
Compile/synthesize the model's cyber part, such that the simulated model and the behavior of the real system coincide.

The main challenge is to guarantee correct timing behavior.

Various Properties of Timing

Hard task
Catastrophic consequence

Firm task
Result is useless, but causes no damage

Soft task
Result has still some utility

Missed deadline

Predictable timing
➔ Guarantee correctness (WCET)

Early miss detection

Immediate miss detection

Late miss detection

Repeatable timing
➔ Same platform: Testability
➔ Changing platform: Portability

Processor frequency

task (clock cycles)

Deadline

Time (measured in e.g., ns)

Precision of timing
➔ Enable accuracy in nano seconds

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Our Approach – Ongoing subprojects

Modeling Languages
Simulink/ Stateflow (Mathworks)
Modelica (Modelica Associations)
Ptolemy II (Eker et al., 2003)
Giotto (Henzinger, Horowitz and Kirsch, 2003)
Modelyze (Broman and Siek, 2012)

Programming Languages
E machine (Henzinger, and Kirsch, 2007)
ptC

- Expose timing constructs

PRETIL

- Abstracting away the memory hierarchy (scratchpad, DRAM etc.)

Assembly Languages
PRET Machine

Compilation of high-level languages with timing semantics

Intermediate language based on LLVM, extended with timing semantics

WCET-aware scratchpad allocation

Precise Clock Synchronization

WCET analysis and WCET-aware compilation

Flexible PRET Machines