Iason F. Vassiliou

EDUCATION:

- **Ph.D.:** EECS Department, University of California, Berkeley, CA, May 1999

  Major: Electrical Engineering - Integrated Circuits & Computer Aided Design

  Dissertation Title: Design Methodologies for RF and Mixed-Signal Systems

  Advisor: Prof. A. Sangiovanni-Vincentelli, Dean P. R. Gray

  Minor: Integrated Circuits for Communications

  Minor: Optimization.

- **M.S.:** EECS Department, University of California, Berkeley, CA, 1995.

  Research Topic: Top-Down , Constraint-Driven Design of a PLL

  Relevant Graduate Classes and Projects: Advanced Analog Integrated Circuits, Advanced Digital Circuits, Advanced Analog ICs for Communications, A/D and D/A Conversion - Design of 2nd Order Sigma Delta A/D, Analysis and Design of High Performance Digital Circuits, Circuit Theory and Computer Aided Analysis, Advanced Digital Signal Processing, Digital Communications, CAD for IC,

  Advisor: Prof. A. Sangiovanni-Vincentelli, Prof. P. R. Gray.

  GPA: 3.8

- **Diploma :** National Technical University of Athens, Greece 1991.

  Major: Electrical Engineering and Computer Science.

  Research Topic: Fuzzy Logic Simulator.

  Advisor: Y. P. Tsividis.

  GPA: 8.50 (out of 10)

RESEARCH INTERESTS

Main interest: Design of Analog and Mixed-Signal Systems. Experience in designing mixed-signal chips (Phase-lock loops, D/A converters, A/D converters, RAMDACs), PCB layout and RF system design.

Design and Methodologies for RF Communications Systems,

CAD for Mixed Signal Systems.

EXPERIENCE:
Academic:

- Spring 1992: Lab assistant, Microelectronics Laboratory, National Technical University of Athens
- Fall 92 - Spring 93: Graduate Student Instructor (UC Berkeley)
- Fall 93 - Spring 99: Graduate Student Researcher (UC Berkeley)

  Hierarchical RF system Design.

Development of new behavioral simulation tools and algorithms. Development of a new RF simulation tool based on Volterra series and Harmonic Balance.

Design of a RAMDAC system. The chip was fabricated and tested. Includes 3 D/A converters and 1 programmable PLL.

Industrial:

- March 1999 - Now: Berkeley Concept Research Corporation, Member of Technical Staff. BCRC is a R & D organization focused on networking.
- Summer 97 -Fall 97 : Cadence Berkeley Labs, Berkeley CA.

  System Design of Voice Mail Pager System (RF/ analog sub-system design)
- Summer 96 : Cadence Design Systems Inc., San Jose CA.

  High-level modeling of RF systems.
- Summer 93 : Internship at Rockwell International, Telecommunications Division (Newport Beach , CA)

  Design of Cyclic A/D converter, behavioral modeling of A/D, D/A converters.

Publications:

- Conferences
  - **Iason Vassiliou** and Alberto Sangiovanni-Vincentelli, "A Frequency-Domain, Volterra Series-Based Behavioral Simulation Tool for RF Systems", In Proc. Custom Integrated Circuit Conference, pages 21-24, San Diego, May 1999.
  - **I. Vassiliou**, H. Chang, A. Demir, E. Charbon, P. Miliozzi and A. Sangiovanni-Vincentelli, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology", In Proc. IEEE/ACM International Conference on CAD-96, San Jose CA, November 1996.
  - A. Demir, E. Liu, A. Sangiovanni-Vincentelli, and **I. Vassiliou**, "Behavioral Simulation Techniques for Phase/Delay-Locked Systems" ,In Proc. Custom Integrated Circuit Conference, pages 453-456, San Diego May 1994.
  - Paolo Miliozzi, **Iasson Vassiliou**, Edoardo Charbon, Enrico Malavasi and Alberto Sangiovanni-Vincentelli, "Use of Sensitivities and Generalized Substrate Models in Mixed-Signal IC Design", DAC 1996, Las Vegas, NV.
- Books
  - Henry Chang, Edoardo Charbon, Umakanta Choudhury, Alper Demir, Eric Felt, Edward Liu, Enrico Malavasi, Alberto Sangiovanni-Vincentelli, **Iasson Vassiliou**, "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits", Kluwer Academic Publishers 1997.

Reviews:

- Peer Reviewer for TCAD (IEEE Transactions on Computer Aided Design)

AWARDS AND MEMBERSHIPS:

- Award of Technical Chamber of Greece (TEE) for academic excellence in academic year 1990 - 1991.
- Student member of IEEE
- Member of Technical Chamber of Greece (TEE)

PERSONAL:

Birth date: October 31, 1968

Citizenship: Greek

ADDRESS:

- Permanent Home Address:

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