SZU-TSUNG CHENG

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FIELDS OF INTERESTS

I am interested in research in all areas of Computer-Aided Design (CAD) of Integrated Circuits and digital systems. My main interest is in the modeling of Hardware Description Languages using automata. I am also interested in the field of combinational and sequential logic synthesis, VLSI circuit design, formal verification, and circuit partitioning.

RESEARCH/WORK EXPERIENCE

1/96–Present: Senior Member of Technical Staff, Cadence Berkeley Laboratories. Have done research/development in the following areas.

- Fast Verilog compilation/synthesis.
- Syntax, semantics, and compilation scheme for HDLs that are suitable for system design.
- The V++ compiler/linker. V++ is a new generation Hardware Design Language.

8/92–12/95: Graduate Student Researcher, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley. Have done research in the following areas.

- Compiling a subset of Verilog hardware description language into timed finite state machines.

OTHER RESEARCH EXPERIENCE

6/92-8/92: NEC C&C Research Laboratory, New Jersy.

- Speed-up a multi-phase retiming algorithm.
- Develop an algorithm, which is applicable to linear circuit, for multi-phase retiming which takes into account the effect of change in delay due to variance of output load.

5/94-8/94: Cadence Berkeley Laboratories, California.

- Verilog to SMV+ compiler.

6/95-8/95: Cadence Berkeley Laboratories, California.

- **vv** - a high speed, high capacity HDL to hardware compiler.

EDUCATION

Ph.D. *Computer Science Division, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley*, California, May, 1998.

Major:	Computers Science
Thesis:	*Compilation, Synthesis, and Simulation of Hardware Description Languages – The Compositional Models of HDL's*
Advisor:	Professor Robert K. Brayton

M.S. *Computer Science Division, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley*, California, May, 1994

Major:	Computers Science
Thesis:	*Compiling Verilog into Automata*
Advisor:	Professor Robert K. Brayton

B.S. *Department of Information Engineering and Computer Sciences, National Taiwan University, Taipei*, Taiwan, R.O.C. , June, 1989. [1]

Major: Computer Sciences

TEACHING EXPERIENCE

1/92–5/92: Graduate Student Instructor for the undergraduate course *"Computer Architecture and Engineering"*, Computer Science Division, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. Responsibilities included instruction, grading and setting examinations and homeworks, and supervising research projects.

RELATED COURSES and PROJECTS

CAD for VLSI - logic synthesis for VLSI, VLSI system design, integrated circuit design, formal verification, physical design;

Computer Science - design and analysis of algorithms, graph theory, probabilistic analysis of algorithms, complexity theory, theory of computation, compiler design, computer architecture and organization, programming language design;

Operations Research - linear programming, non-linear programming, and combinatorial optimization, network flow.

DESIGN PROJECTS INVOLVED

- VIS [7,8].
- HSIS [9] and a graphical user interface for HSIS.
- vl2mv – a Verilog to timed FSM compiler.
- Design of a FPGA chip.
- Superscalar processor (superscalar DLX) simulator as well as a new caching scheme for processor of this kind.
- General purpose Neural network simulator.

[1] I got the first in the ranking among the class.

- Compiler-design for a subset of the ADA-programming language.
- C informatin abstrctor - A system used to extract data and control flow as well as cross-reference between routines so as to facilitate project management.
- C^3I system (command, control, communication and intelligence) - Through digital communication, the system is used to collect/show real-time troop information in the battlefield to help a commander make desision.

Awards and Honors

- The first in the ranking among the class during the undergraduate study at the Depart of Computer Science and Information Engineering, National Taiwan University.
- Seven times the Book Coupon Awards from National Taiwan University. Only students among the top five percent are entitled to the award.
- Best Paper Award for "Cycle Simulation Semantics of Verilog and SMV: Cobra from Concept to Simulator", Cadence Technical Conference '96.
- Special Achievement Award from Cadence Design Systems, Inc., 1997.

PUBLICATIONS

[1] Szu-Tsung Cheng, "Compilation, Synthesis, and Simulation of Hardware Description Languages – The Compositional Models of HDL's", PhD thesis, University of California, Berkeley, 1998.

[2] Szu-Tsung Cheng, Patrick C. McGeer, Tom Truman, Patrick Scaglia, Alberto Sangiovanni-Vincentelli, Robert K. Brayton, "Finite State Machine Communication in V++", Cadence Technical Conference, 1998.

[3] Szu-Tsung Cheng, Patrick C. McGeer, Fabio Somenzi, Patrick Scaglia, "Object-Oriented Simulation of Hardware Descriptions: Solving the Namespace Problem in a Pure Hardware Language", Cadence Technical Conference, 1998.

[4] Szu-Tsung Cheng, Patrick C. McGeer, Mike Meyer, Tom Truman, Alberto Sangiovanni-Vincentelli, Patrick Scaglia, "The V++ System Design Language", Design, Automation and Test in Europe, 1998.

[5] Szu-Tsung Cheng, Alexander Saldanha, Patrick C. McGeer, Patrick Scaglia, Robert K. Brayton, "The Synchronous Semantics of Verilog: A Functional Interpretation of Verilog Programs", Cadence Technical Conference, 1997.

[6] Szu-Tsung Cheng, Patrick C. McGeer, Mike Meyer, Alberto Sangiovanni-Vincentelli, Patrick Scaglia, "The V++ Systems Design Language", International Workshop on Logic Synthesis, 1997.

[7] Szu-Tsung Cheng, Robert K. Brayton, "Synthesizing Multi-Phase HDL Programs", Proceedings of International Verilog Conference, 1996.

[8] Szu-Tsung Cheng, Patrick, C. McGeer, Kennith L. McMillan, Alexander Saldanha, Alberto Sangiovanni-Vincentelli, Patrick Scaglia, "Cycle Simulatioin Semantics of Verilog and SMV: Cobra from Concept to Simulator", Cadence Technical Conference, 1996.

[9] Szu-Tsung Cheng, Robert K. Brayton, Gary York, Katherine Yelick, Alexander Saldanha, "Compiling Verilog into timed Finite State Machines," Proceedings of International Verilog Conference, 1995.

[10] Robert K. Brayton, Gary D. Hachtel, Alberto Sangiovanni-Vincentelli, Fabio Somenzi, Adnan Aziz, Szu-Tsung Cheng, Stephen Edwards, Sunil Khatri, Yuji Kukimoto, Abelardo Pardo, Shaz Qadeer, Rajeev K. Ranjan, Shaker Sarwary, Thomas R. Shiple, Gitanjali Swamy, Tiziano Villa, "VIS: A System for Verfiication and Synthesis", Proceedings of the Conference on Computer Aided Verification, New Brunswich, MJ, July 1996.

[11] Robert K. Brayton, Gary D. Hachtel, Alberto Sangiovanni-Vincentelli, Fabio Somenzi, Adnan Aziz, Szu-Tsung Cheng, Stephen A. Edwards, Sunil P. Khatri, Yuji Kukimoto, Abelardo Pardo, Shaz Qadeer, Rajeev K. Ranjan, Shaker Sarwary, Thomas R. Shiple, Gitanjali Swamy, "VIS", FMCAD'96.

[12] Adnan Aziz, F. Balarin, S. T. Cheng, R. Hojati, T. Kam, S. C. Krishnan, R. K. Ranjan, T. R. Shiple, V. Singhal, S. Tasiran, H.-Y. Wang, R. K. Brayton, and A. L. Sangiovanni-Vincentelli, "HSIS:A BDD-Based Environment for Formal Verification", 31st ACM/IEEE Design Automation Conference.

[13] A. Ranade, S.-T. Cheng, E. Deprit, J. Jones, S.-I. Shih, "Parallelism and locality in priority queues", the Proceedings of the Sixth IEEE Symposium on Parallel and Distributed Processing, Dallas, October 26-29, 1994.

[14] Adnan Aziz, F. Balarin, S. T. Cheng, R. Hojati, T. Kam, S. C. Krishnan, T. R. Shiple, V. Singhal, H.-Y. Wang, R. K. Brayton, and A. L. Sangiovanni-Vincentelli, "Formal Design Verification of Degital Systems", SRC Techon'93.

[15] Felice Balarin, Robert K. Brayton, Szu-Tsung Cheng, Desmond A. Kirkpatrick, Alberto L. Sangiovanni-Vincentelli, Ephrem Wu, "A Methodology for Formal Verification of Real-Time Systems", Memorandum UCB/ERL M95/11, University of California at Berkeley, 1995.

[16] Szu-Tsung Cheng, "Compiling Verilog into Automata", Master Thesis, May, 1994.

[17] Ja-Ling Wu, Szu-Tsung Cheng, "A Neural Network Simulating System", The Computer Journal, vol. 34, No. 1, 1991.