An Implementation of a Differential Transconductance Amplifier for a 13 Bit A/D Converter

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This report summarizes an implementation of a fully differential transconductance amplifier intended for a 13 bit A/D converter. In this implementation, a telescopic cascode first stage, a common-source second stage and a static Common Mode Feedback circuit are used to achieve a open-loop gain of over 60000, a close-loop dynamic range of 80.08 Decibel and a settling time (0.01%) of < 100ns. Aside from the often-used pole splitting compensation, techniques such as a dynamic current source and a current-pulse generator are exploited to improve the settling while minimizing the total power consumption. As a result, a worst-case power of 1.6mw (excluding the biasing circuit) is measured by using a HSPICE simulator.

1.0 Introduction

In this project, we adopted a top-down approach for a OTA design: we made high level decisions to reduce the solution space down to a reasonable amount,pinned down individual issue and devised specific solutions to address each of them. Starting with the sturcture of our gain stages, first we read through several research papers to search for different circuit configurations and topologies. Then, we carefully examined the available options according to the given specifications and based on a blend of common sense and intuition, we were able to quickly rule out most of unsuitable options. For example, a single stage approach could achieve a gain of over 10000, but did it at a cost of output range; therefore, a two stage implementation was singled out. Also, we rejected folded cascode first stage because it had three pairs of devices contributing noise to the output and it has more devices to induce output offset. As firm believers of the saying ”Simpler is better”, we finally decided to use a simple two-stage configuration.

Our first stage was a telescopic cascode and our second stages used a pair of common sources. A pair of compensation capacitors were inserted between the output nodes of the first and second stage. A quick estimate allowed us to allocate equal currents of the first stage and each branches of the second stage because, apparently, second stage needs to drive more load than the first stage does.

A simple biasing scheme was also quickly sketched out afterwards. In our biasing network, a pair of resistors were used to bias two pairs of devices in the first stage around half way between the Vdd and ground. Although resistors are, in general, expensive to build and difficult to be precise, in our particular case, we claim it less a problem: first, the exact voltage output produced by the resistor does not set the biasing current and needs only to be within a range in which the devices on the top and the bottom is ensured to operate with the saturation region. errors; secondly, we believe that a very good biasing network alone is worth the effort of a whole final project, therefore, we would rather focus on the implementation of the core amplifier.

The next decision was about the common mode feedback circuit and two available options were a dynamic CMFB and a static CMFB. Ideally, dynamic CMFB dissipates zero static power and is relatively simple to implement, but requires the availability of the inverting common mode output signal which is not the case for our two stage OTA. If we were to stick with the dynamic style, a pair of inverters would be needed to provide such an inverting common mode output and the static power is unavoidable. As a result, we adopted a static CMFB implementation.

After putting pieces of thoughts and ideas together, we had a much clear view of what we were going to build. Based upon what was given, it was necessary to have a idea what kind of high level tradeoffs were involved and we summarized our results in Table 1.

TABLE 1. Tradeoffs: At a Hige Level

	Increase output swing	reduce noise	reduce settling time	increase open loop gain	increase phase margin	reduce power
device size	increase W/L	increase L, reduce W/L	decrease (parasitic)	increase W/L		
Cc		increase	reduce		increase	
Cs		increase	reduce		reduce	
Nf		reduce				
I_{bias}	reduce		increase	reduce		reduce

From Table 1, the only option we had to reduce the power was to reduce total biasing current, which would also help the open loop gain and the range of output swing. The only thing that reducing I_{bias} hurt was the settling time and it seemed that we could reduce Cc or Cs , upsize the critical devices or reduce the noise factor (which also involved device sizing). Overall, our strategy was to reduce I_{bias} and Nf, increase W/L, while maintaining a suitable value for Cc and Cs.

Also, we pinned down a particular design issue and devise a specific solution to tackle this problem To improve the slew-rate, we put a circuit which we call a current pulse generator by every current source and turn it on right after every sampling for a few nano seconds and then turn it off. Our setting time was significantly imporved, allowing us to minimize the steady state current in our circuit. Since A/D converters are clocked anyway, our current pulse generator are also clocked by these clocks. The power consumption by these dynamic current sources is minimal since they are on for only a few nano second during each clock cycle.

As our result turned out, our early design decisions help us find an optimum path in meeting all the specs while minimizing the total power dissipation.

2.0 Outline

2.1 Approach to minimize power consumption

Aside from aforementioned reasons to reject a folded cascode approach, power dissipation presents yet another problem of a folded cascode. Under comparable situations, a fold cascode would require 4 branches to be operational whereas a telescopic cascode only needs 2 branches.

Also, we reduced the current of the common mode feedback circuit by ratioing the size of certain critical devices.

But the most important aspect of minimizing power would have to be the minimizing the output noise. The logic lies as follows:

1. Reduce the noise so that we have extra room to spare on the dynamic range.
2. Reduce Cc and Cs so that the noise increases but still within budget for dynamic power, but this will reduce the settling time.
3. Reduce Ibias so that the settling time would increase but still less than 100 ns
4. To complete this logic, a loop would be directed back to step1, until no further improvements could be "squeezed" out, then exit the loop and the project is finished.

Because we also used a "current pulse generator" circuit to help the slew, we would have just added another dimension for the previous logic "loop". Upto this point, we strongly felt that, just like many other engineering problems, designs of this sort could be formulated into a search problem: to search for an optimum point inside a multi-dimensional solution space. Software programs could be created to automate the search process and also, there are ongoing research projects aiming at improving the computational efficiency of the design[1].

2.2 Circuit schematics with device sizes and and important biasing currents and voltages.

A circuit schematic showing the gain stages, biasing network and a CMFB network is on the following page. Please notice five transistors in parallel with all "current source" transistors, they require control signals generated from a "current pulse" generator.

Also due to the space limitations, we were not able to label the Gm and W/L for all the critical devices, but we enlisted them in Table 2.

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Differential Amplifier with Current Pulse Generator

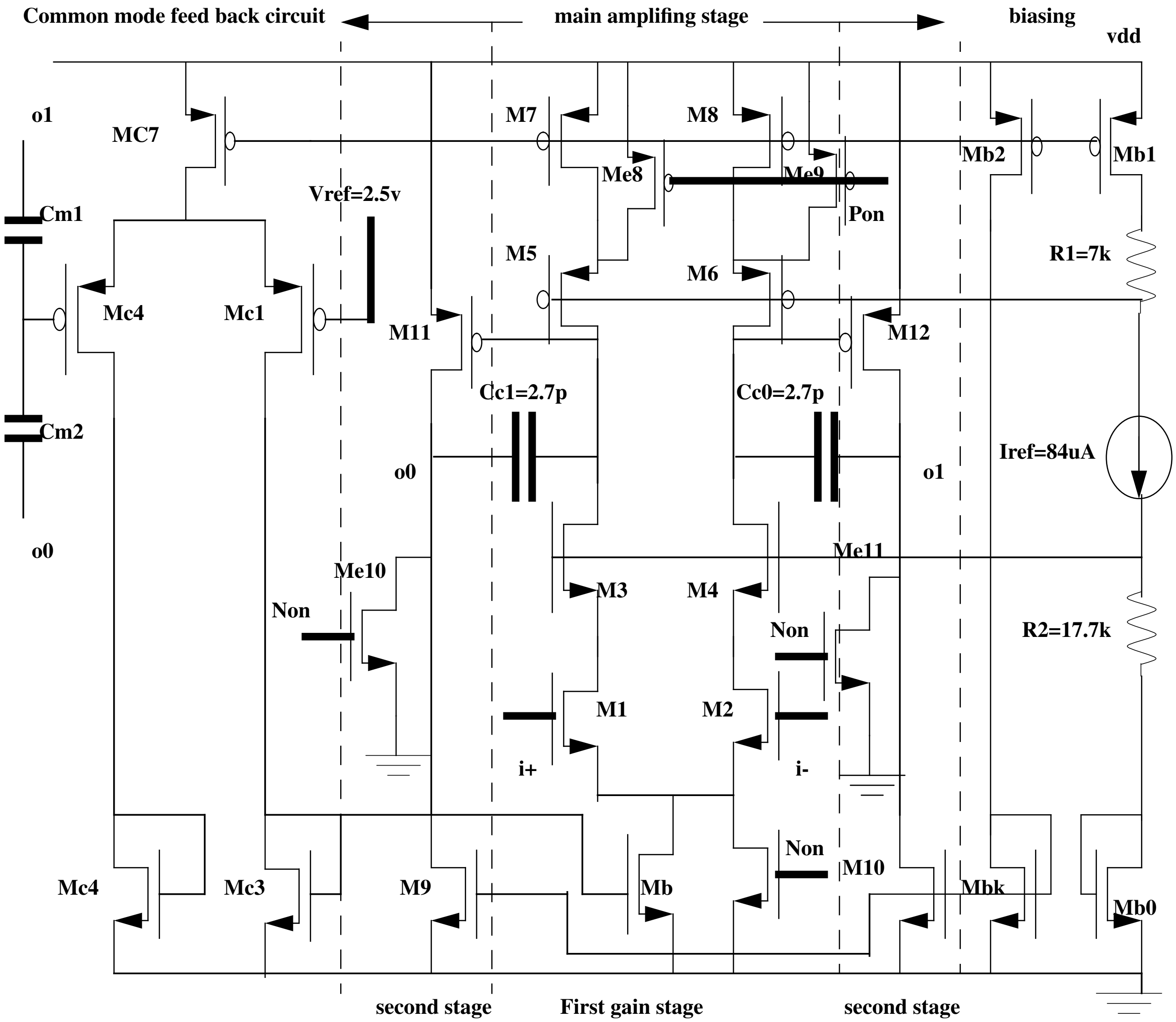

FIGURE 1. Main Circuit Configuration (not including current pulse)

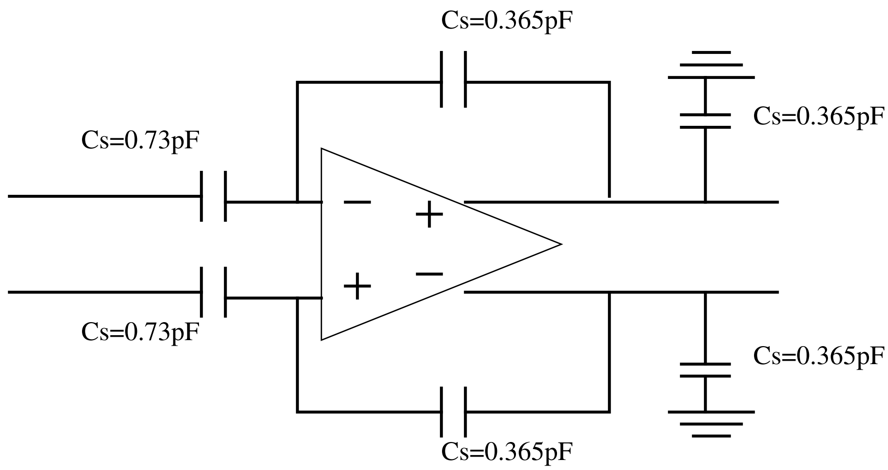

FIGURE 2. Close Loop Circuit

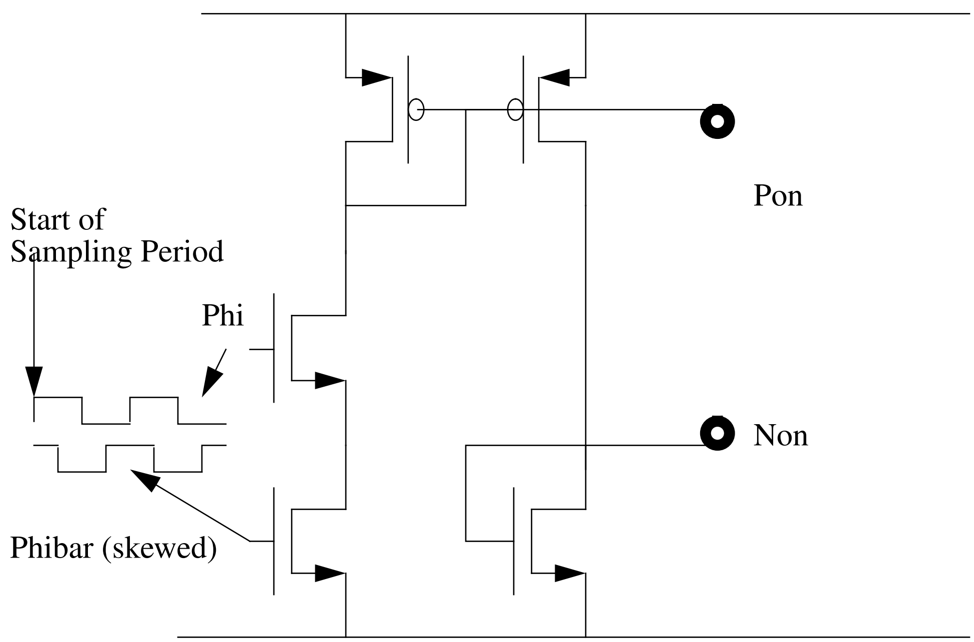

FIGURE 3. Current Pulse Generator

TABLE 2. Summary of Devices' Properties

Device Nmae	Device Size (W/L)	Gm(s) (slow/nom/fast)	Vd(sat)(volt) (slow/nom/fast	Important Current (A) (slow/nom/fast)(Ids)
M1	80/1.2	970u/1.04m/1.1m	120.1m/112.7m/104.7m	78.1u/79.07u/79.96u
M2	80/1.2	970u/1.04m/1.1m	120.1m/112.7m/104.7m	78.1u/79.07u/79.96u
M3	80/0.6			
M4	80/0.6			
M5	180/1.2			
M6	180/1.2			
M7	180/1.2	768.8u/822.7u/885.4u	157.2m/144.7m/131.8m	78.1u/79.1u/79.96u
M8	180/1.2	768.8u/822.7u/885.4u	157.2m/144.7m/131.8m	78.1u/79.1u/79.96u
M9	90/1.2			
M10	90/1.2			
M11	300/0.6	2.29m/2.64m/3.17m	118.1m/104.9m/91.2m	185u/192u/199.5u
M12	300/0.6	2.29m/2.64m/3.17m	118.1m/104.9m/91.2m	185u/192u/199.5u
Mb	192/0.6			155.6u/158.2u/159.9u
Mb1	180/1.2			
Mb2	360/1.2			
Mb0	60/0.6			
Mbk	90/1.2			
Mc7	40/1.2			16.28u/16.7u /17.08u
Mc1	4/0.6	53.7u/49.7u/36.7u		
Mc2	4/0.6	53.7u/49.7u/36.7u		
Mc3	12/0.6			
Mc4	12/0.6			
Me1	30/3			
Me2	9/3			
Me3	9/3			
Me4	10/3			
Me5	30/3			
Me6	10/3			
Me8	10/3			
Me9	10/3			
Me10	10/3			
Me11	10/3			

3.0 Operation of Building Blocks.

3.1 Performance summary tables:

TABLE 3. Close loop characteristics

device model	settling time	noise(uV)	dynamic range	static power(excluding bias)	dynamic power	total power
slow	<100 ns	161.8449	80.0044	1.53mW	0.04mw	1.57mW
nominal	<100ns	160.1405	80.1508	1.58mW	0.04mw	1.62mW
fast	<100ns	158.8463	80.3325	1.63mW	0.04mw	1.67mW

TABLE 4. Open loop characteristics

model	1st stage gain	2nd stage gain	overall gain	overall gain at v_{dm}=2.3	1/f=3 phase margin
slow	5.08×10^3	37.8	1.89×10^5	1.82×10^5	72^o
nominal	4.10×10^3	29.7	1.18×10^5	1.16×10^5	75^o
fast	3.09×10^3	22.8	6.89×10^4	5.74×10^4	77^o

3.2 First stage

- As mentioned before, noise factor Nf is critical to the total output thermal noise and for the case where the output loading is negligible, the output thermal noise is proportional to the square root of Nf.
- To reduce the flicker noise, it is also important to increase both W and L of critical devices (M1, M2 & M7,M8).
- Since the spice model we use does not work well for channel lengths about 0.6um, we can only scale Ls of M7,M8 to 1.2um. In fact, L of M7and M8 should be as bigger as possible because it helps reduce both thermal (smaller Nf) and flicker noise.
- The transconductance should also be positioned correctly in order to push the unity gain frequency to a higher frequency while not sacrificing too much phase margin.

3.3 The second stage

The second stage is just a very simple common source stage with an active load. In the beginning we used the nmos for the common source stage and the pmos for the load. We discovered later that since the input devices of the first stage were nmos's, it was nearly impossible for the output of the first stage to reach the high gain input region of the second stage, which is close to Vth if pmos load were used for the 2nd stage, without pushing the nmos's of the first stage into the triode region. So we decided to reverse the second stage and use nmos load instead. We were able to achieve double digit gain at the second stage.

The main purpose of the second stages, besides amplifying the signal, is to drive the external capacitive load. As a result, the biasing current is twice the amount of that in a single branch of the first stage.

3.4 Common mode feedback

If the common mode output is too high, the voltage at the gate of mb should be lowered so that the common mode level of the first stage output is raised, and vice versa. Thus we need a common mode feedback circuit that performs an inversion function. That is exactly why we used a differential pair. The 2 capacitors in effect act as a divide-by-two circuit. The feed the average value of the two output of the amplifier to the common mode feedback circuit. The desired common mode output voltage, 1.5, is connected to the other input devide of the diff pair. A high common mode output pushes all the current to the left side, thus raising bias0.

The size of the input pair plays a subtle role in the settling time of the close loop.

3.5 Compensation capacitors

Both the first stage and the second stage of the amplifier have relative high impedance, therefore, the close loop frequency response would degenerate and become unstable at the desired circuit operating frequency. Since various methods had been introduced during the course, we chose to put the compensation capacitor between the two output stages and by doing that, we are able to split the poles apart and improve the phase margin. Notice that no “nulling resistors” were added in series with the compensation capacitors and this is because the left pole zero, as described in G&M, is way out of the frequency scope of our interest.

3.6 <u>Current Pulse Generator</u> Vs. <u>Dynamic Current Source</u>

During the slewing period, the output settling is limited by the biasing current. After the slewing period, however, the settling goes back to the old “R*C” time constant relationship. By identifying the fact that increasing the biasing current during the linear settling period at the cost of extra static power dissipation does little to the overall settling rate, we were able to devise two new circuits both aiming to reduce or even eliminate the static power dissipation during the linear settling period.

The first circuit, as depicted in Figure 4, is called a “dynamic” current source. During the rising period of the clock signal, a capacitor is charged up to Vdd whereas the rest of the circuit is shut off; when the clock makes a high to low transition, the rest part of circuit gets turned on and starts to discharge the capacitor thru a “diode” connected transistor. By properly ratioing the W/L of the “diode” connected transistor and external “target current source” transistors, we are able to run a current of abitrary amount thru the “target current source” transistor to help the slew. The transient wave form of the “remote” current, however, follows exactly that of the diode transistor. Eventually, the capacitor will be discharged to approximately the threshold value of the “diode” connected transistor and this, in turn, would turn off the “target current source”. It is important to notice that “target current sources” contribute either common mode noises or noises during the “on” period. Also, due to the symmetrical structure of the OTA, when the input differential mode input signal stays at zero, the output of the OTA would remain zero (the injection of the current would only cause the common mode pertubation).

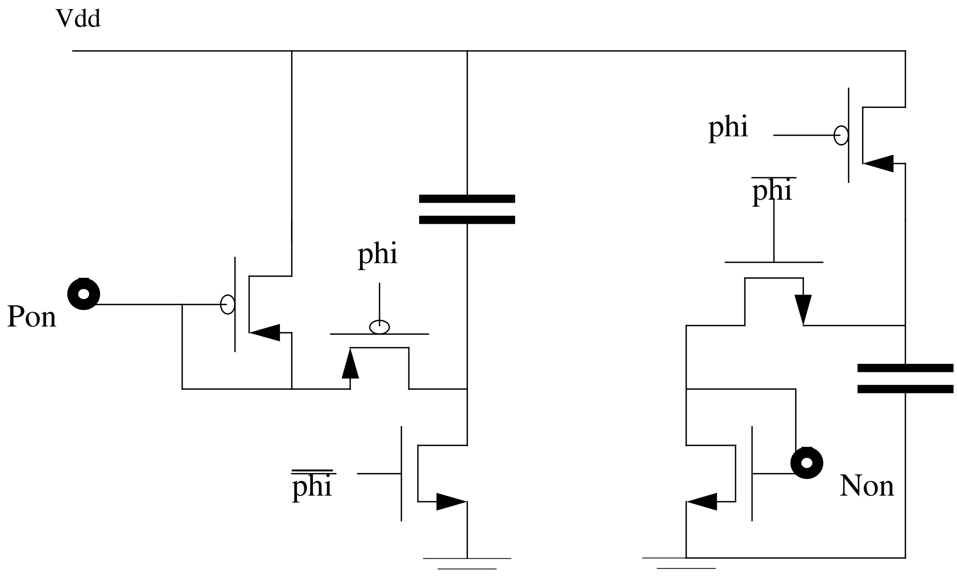

FIGURE 4. A Dynamic Current Source

To test the circuit, we add it into spice netlist and simulate the transient response. The outcome seems encouraging-- we were able to cut the non-linear settling time to a third of that experienced by a “helpless” amplifier. The implication of this is clear- to achieve the same amount of settling time period, we could run much smaller biasing current across the circuit while still maintaining a reasonably large capacitor for the purpose of reducing the thermal noise value.

There is one problem making this circuit less attractive. Suppose the output differential mode signal is large, or in other words, the two output nodes stay at both rails, and assume this signal remains constant when the clock ticks, there will be a current pulse injecting into the circuit and causing the output differential mode signal to deviate from the orginal value. To ensuring a A/D converter to sampling the right value, we must expect such a deviation to converge to a value of within 0.01% of the original value in less than 100ns(Figure 5, Figure 6). Therefore, we have to make sure that the discharging process of capacitors to be fast enough so that “helper” currents could disappear fast enough, which conflicts the desirable, longer period of “slewing” period. What we want is a current pulse generators which produces a current pulse of a given magnitude lasting for an adjustable period of time.

The second circuit e came up with does exactly that. Shown in Figure 3b, the circuit requires Phi and $\overline{\text{Phi}}$ to be skewed so that the two NMOS device would be conducting simultaneously in a short period of time. During that period, the current flows thru a diode connected PMOS device which mirrors currents in devices with gates tied to it.

Overall, we are able to use a large Cc to reduce total output noise while still meeting the specs on the settling time.

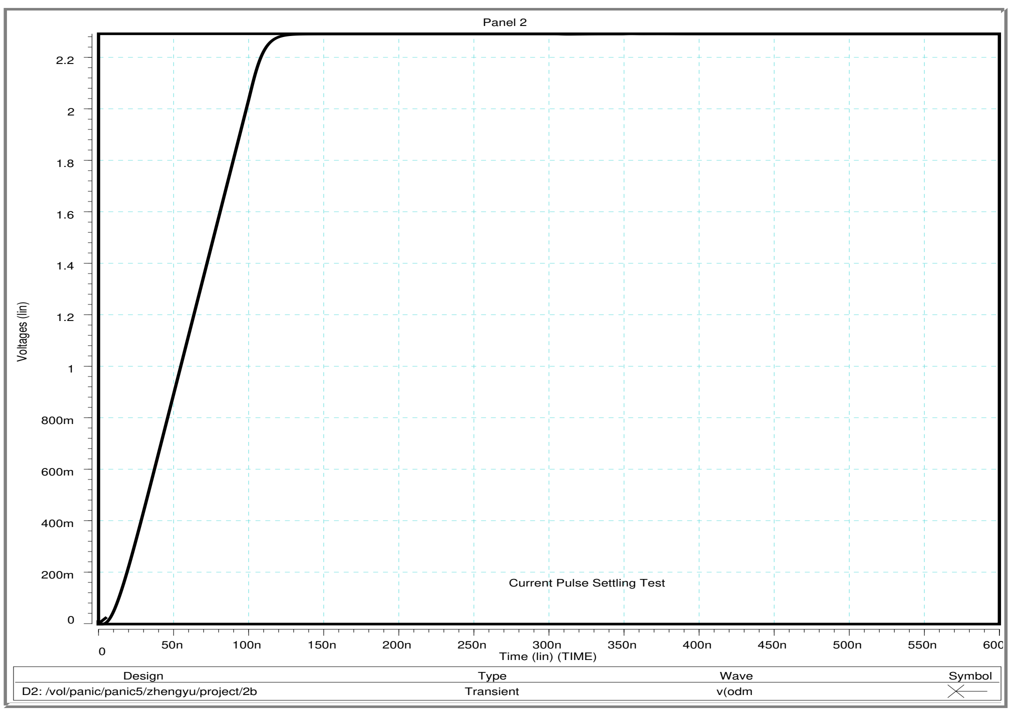

FIGURE 5. Settling Test of the Current Pulse Generator with Zero Output Change

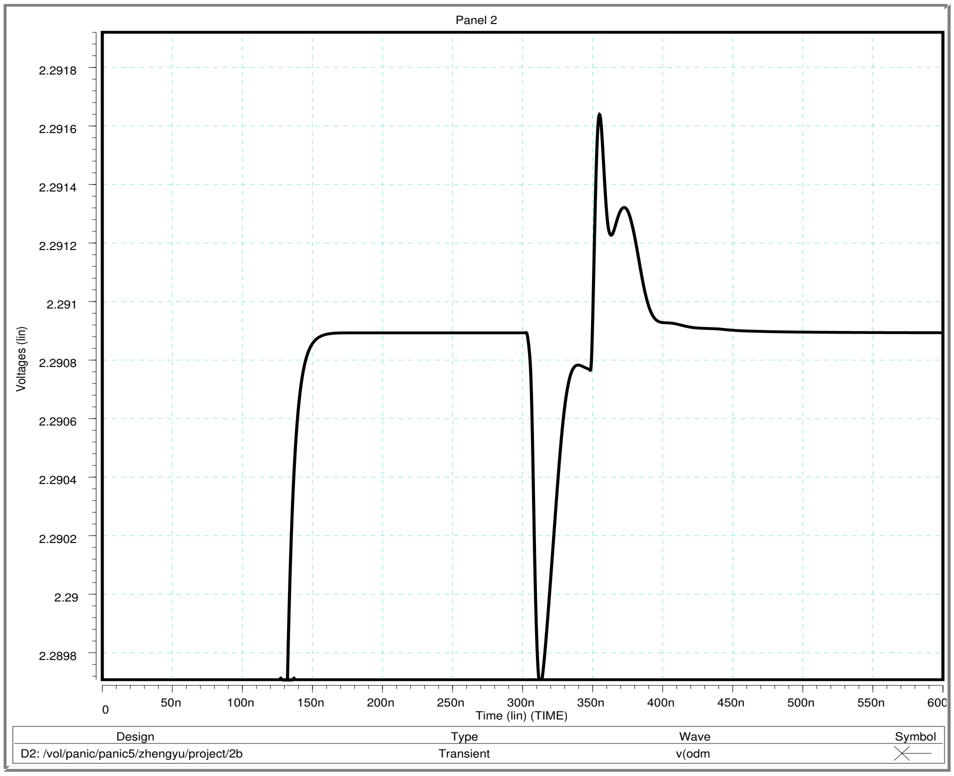

FIGURE 6. Zoom-in view of Figure 5 (Clock starts @ 300 ns)

4.0 Results and Supporting Details.

4.1 Open Loop DC Transfer Characteristics (Figure 7)

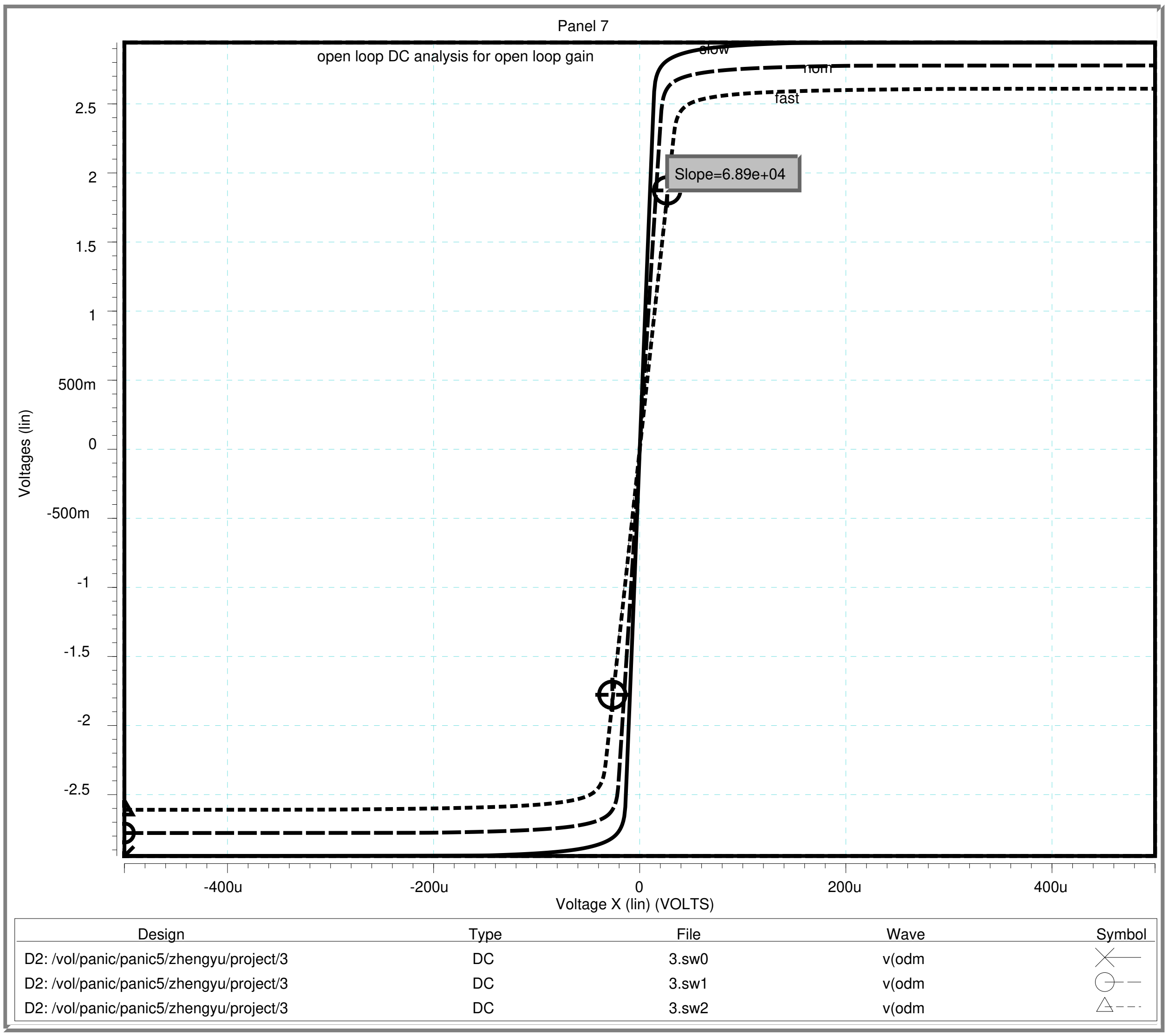

FIGURE 7. Open Loop DC Transfer Characteristics (<u>Showing a worst case gain of 69000)</u>

4.2 Verify Output Range (Figure 8)

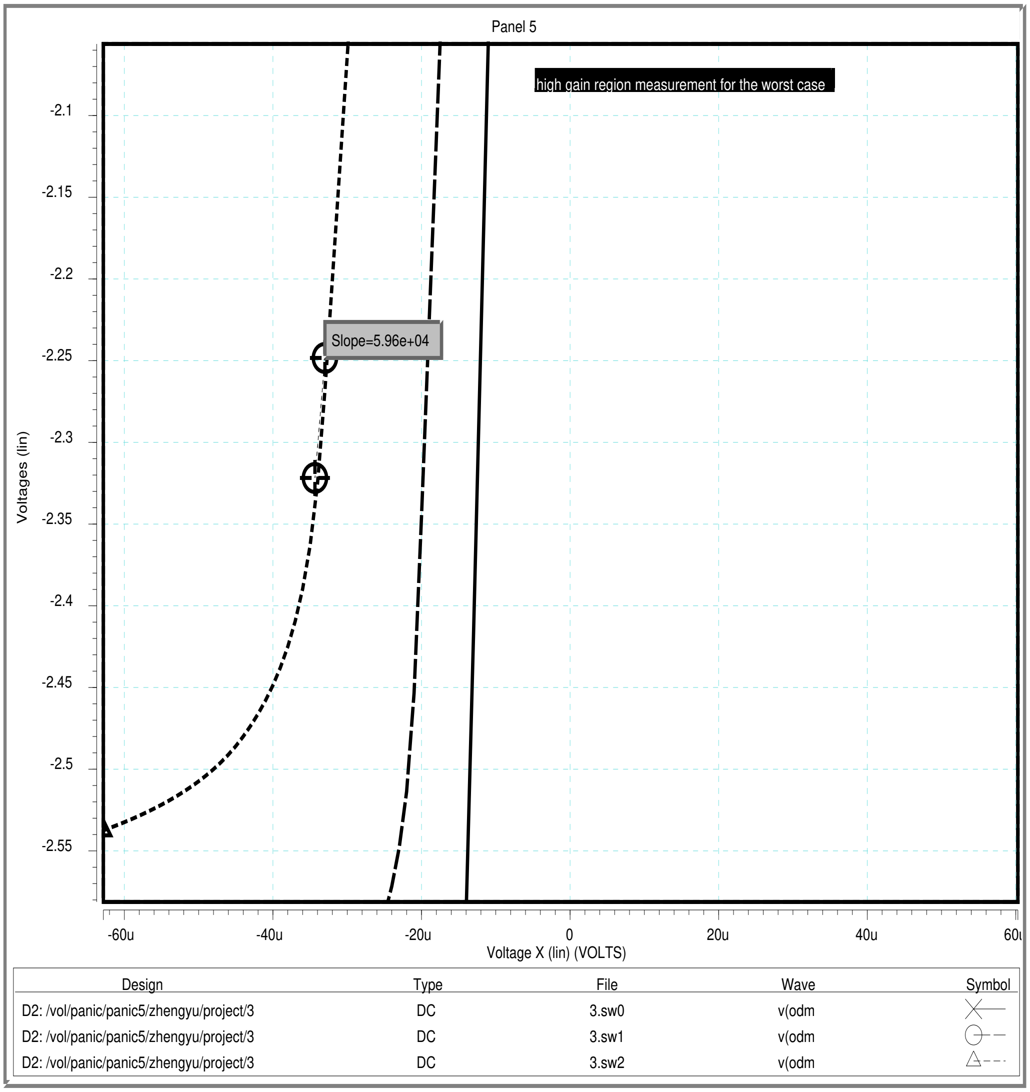

FIGURE 8. Output at 2.3 Volt with a Gain of 69000 (at high gain region)

4.3 Open loop Frequency Response (Figure 9)

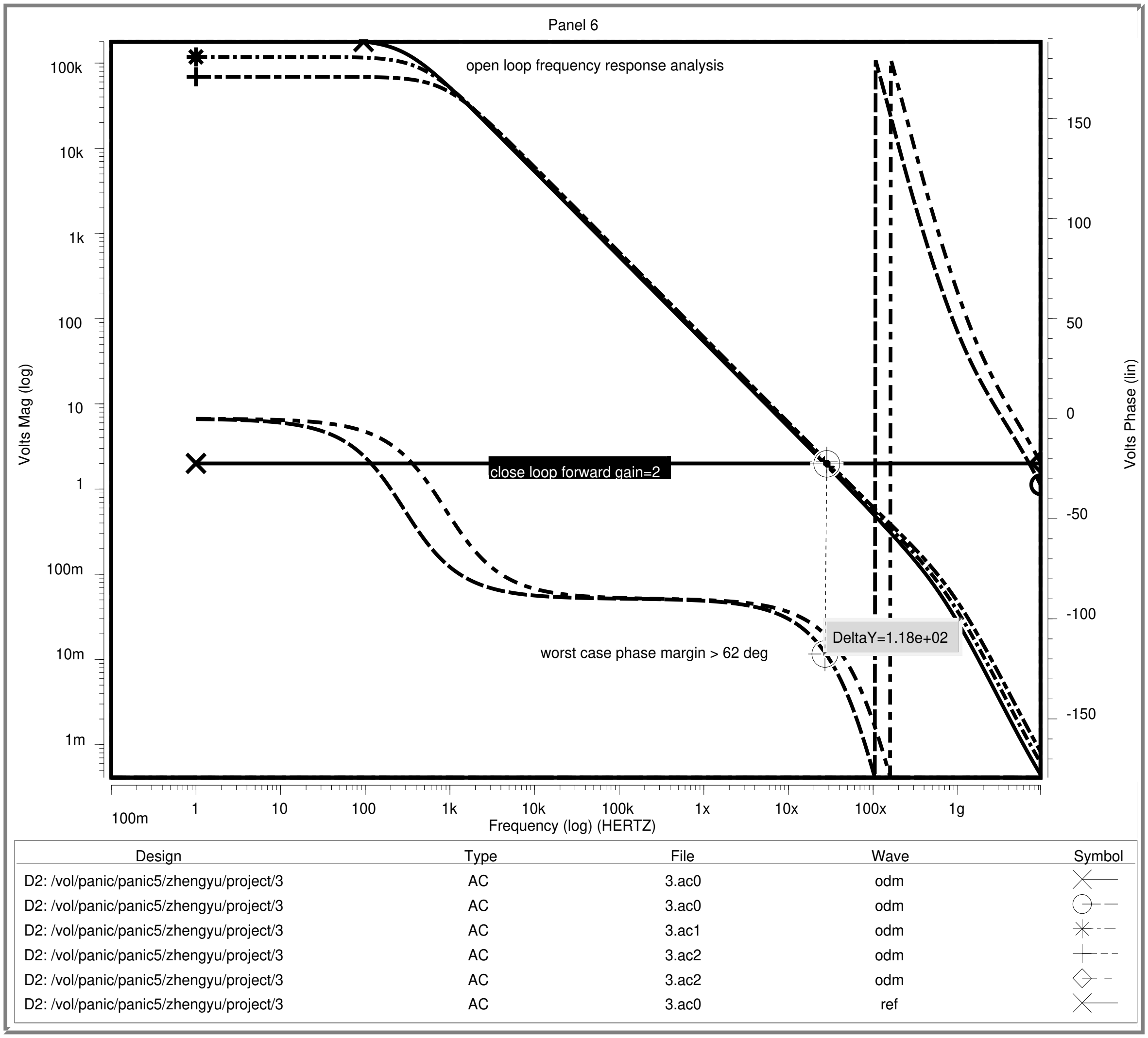

FIGURE 9. Open Loop Response

4.4 Close Loop Transient Analysis with 2.3 Volt Step Output (Fig 10.11)

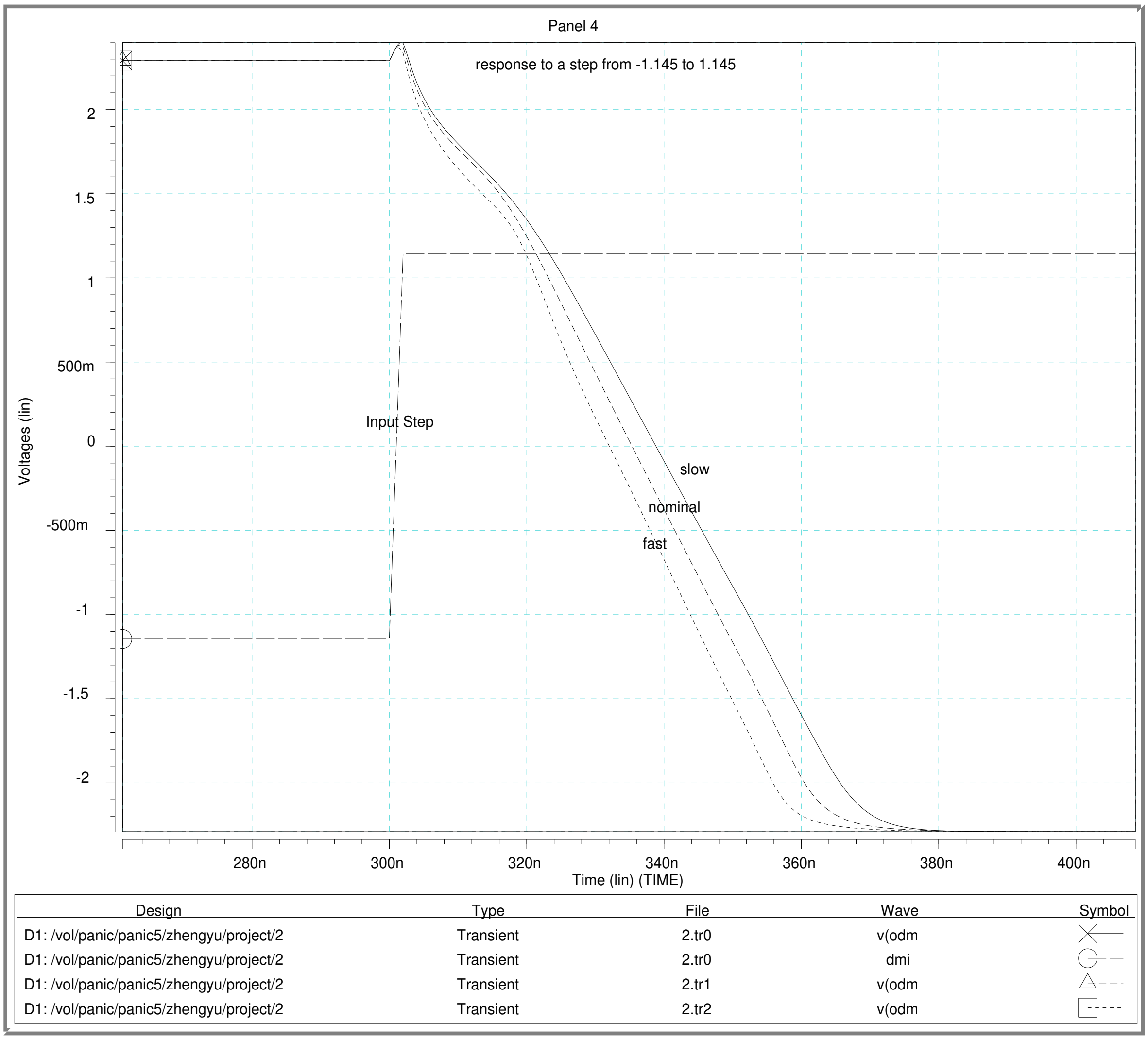

FIGURE 10. Close Loop Transient Analysis with 2.3 Volt Step Size output

f

Fast devices have lower vt's, thus they consume more power.

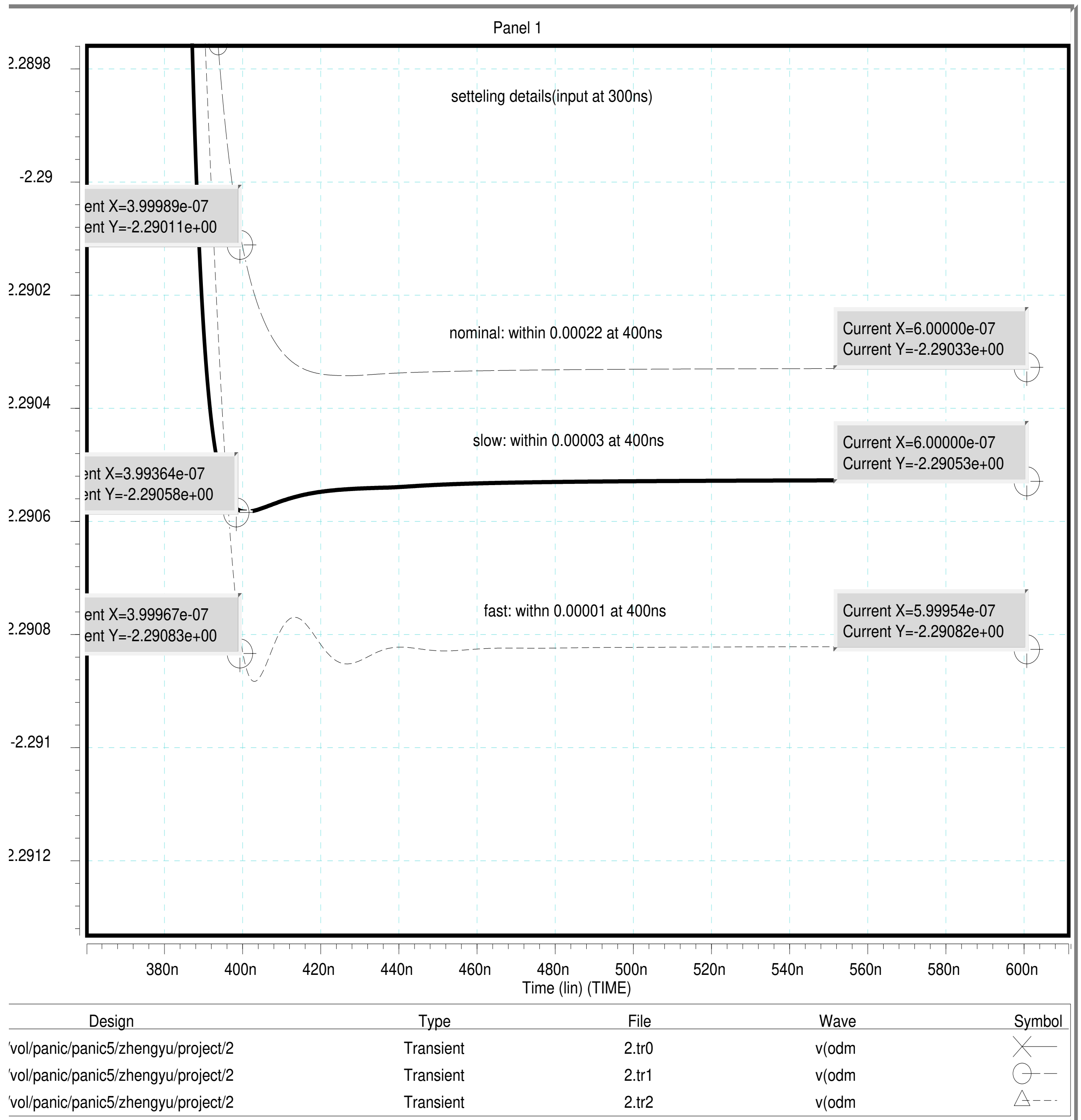

FIGURE 11. Zoomed-In view of Figure 10

4.5 Noise Spectrums of Critical Devices

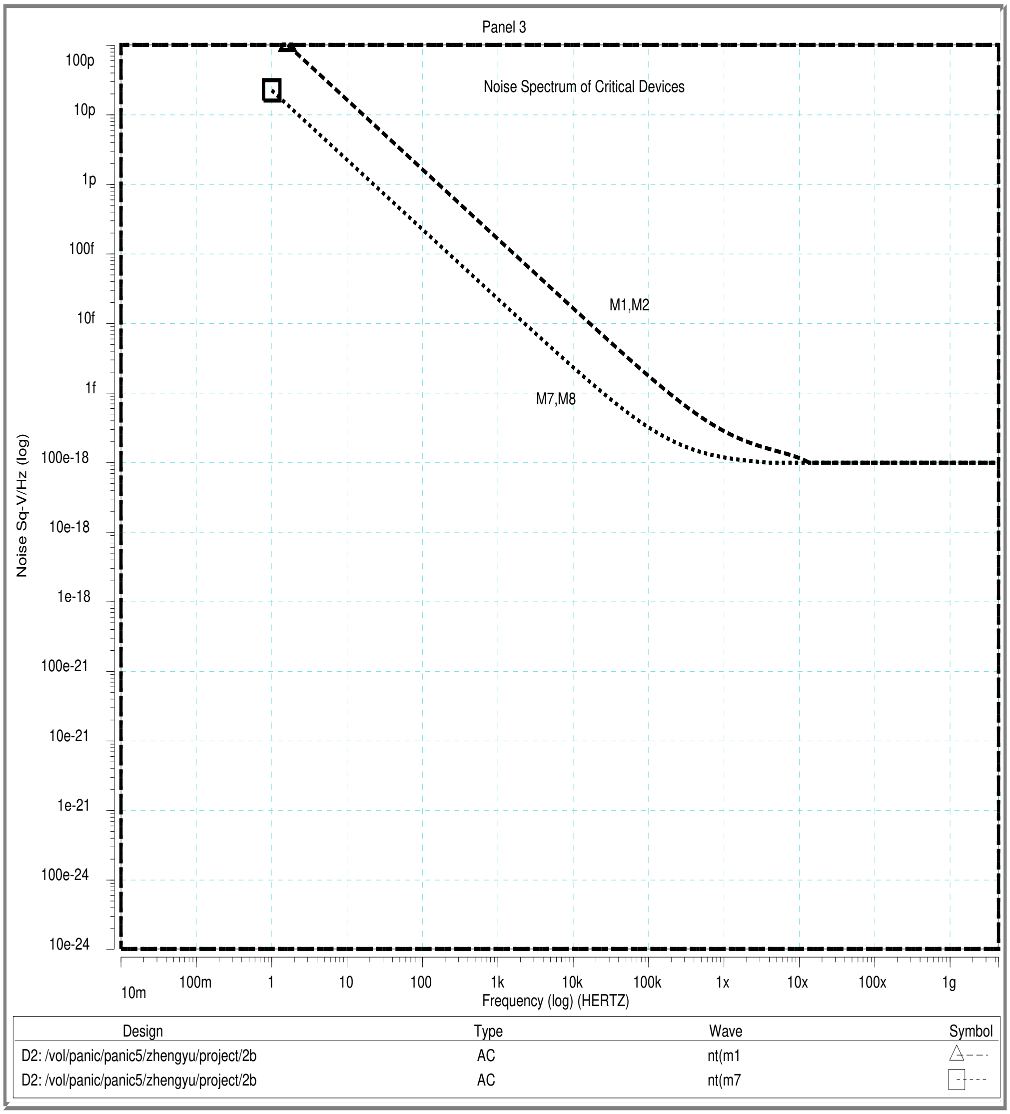

FIGURE 12. Noise Contribution from the Critical Devices

4.6 Power Estimation

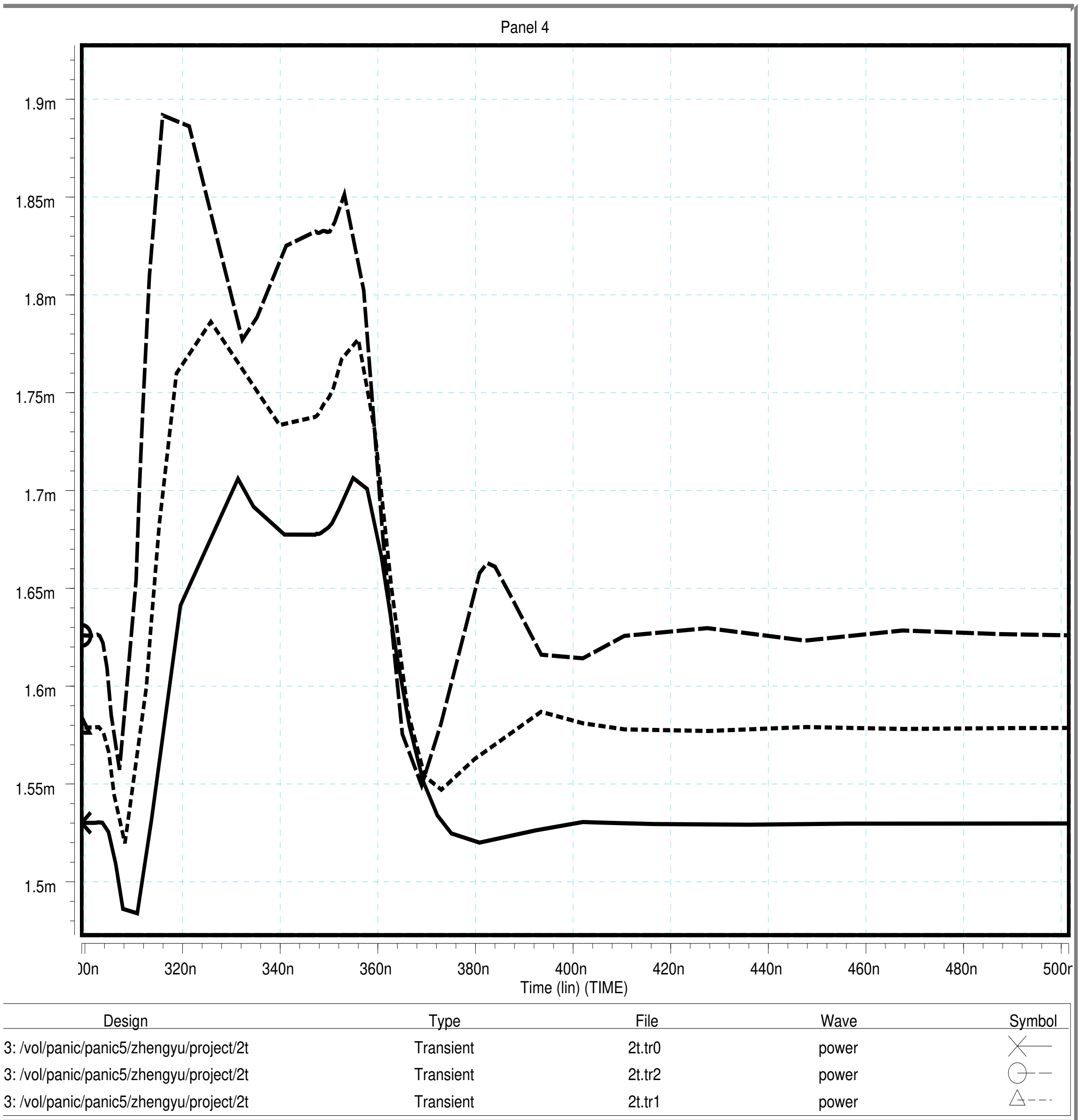

FIGURE 13. Power Estimation of the Close LoopCircuit (P(wosrt)=1.67mw)

4.7

plot of zoom-in's

5.0 Why our desing is outstanding

We were able to meet all the specs with only 1.0 mw of power.