UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Term Project	**EECS 240**
B. E. BOSER	**Due Friday, December 5, 1997**	**FALL 1997**

Objective

You are to design a fully differential transconductance amplifier to be used in the first stage in a pipelined 13-Bit A/D converter. Figure 1 shows conceptual diagram of the amplifier and its use as a gain stage.

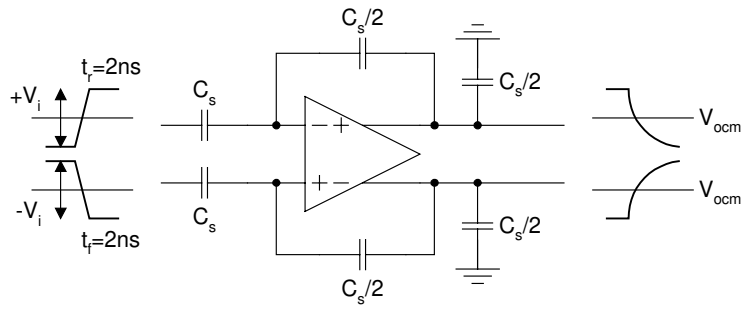

Figure 1 Conceptual diagram of amplifier configured as gain stage.

The table below summarizes the design specifications. The key design objective is minimizing the power dissipation while meeting all design requirements. The circuit is to be fabricated in the EECS 240 CMOS technology. Check the performance with slow, nominal, and fast SPICE.

Supply, V_{DD}	3 V
Dynamic range, DR	≥ 80 dB
Open-loop voltage gain, A_{v0} (V_{od}=max)	≥ 10,000
Settling accuracy, ε	≤ 0.01 %
Settling time, t_s	≤ 100 ns

The dynamic range, DR, is defined as

$$DR = 10\log\left(\frac{P_{peak-signal}}{P_{noise}}\right)$$

and measured at the output of the amplifier. The peak signal power, $P_{peak\text{-}signal}$, is the power of the maximum sinusoidal signal that does not overload the amplifier. The noise, P_{noise}, is the total noise at the amplifier integrated from 1Hz to "infinity". The justification for the upper integration limit is the presence of switches in the real circuit, which cause all noise to alias into the signal band. You are free to choose an optimal tradeoff between signal-range and capacitor size to meet the dynamic range specification.

You must design the entire circuit including common-mode feedback circuit and biasing network with the exception of one supply independent reference current source. This is to keep things simple—in practice

you would have to design this circuit as well. If you use a dynamic common-mode feedback circuit, you may assume it has been initialized properly prior to applying the input step to the amplifier.

Result

Document your results in a written report. It should be *concise* summary of your work and should highlight the most important features of the design. Explain clearly why you chose a particular solution over an alternative and *demonstrate convincingly* how your design meets all requirement. You may add appendices to expand upon significant aspects of the design, or provide supporting calculations and simulation results. Treat the appendices as references within the main text of the report.

The following are crucial parts of the report:

- A brief introduction describing your design, justifying your decisions, and comparing your approach to alternatives.
- An outline of your design, including your approach to minimizing the power dissipation, circuit schematics with device sizes and important biasing currents and voltages. Mark the $V_{d(sat)}$ and g_m for all critical devices in the schematic.
- Comments on the operation of all building blocks, and a performance summary table verifying that all design criteria are met under nominal and worst-case conditions.
  Investigate potential concerns of your particular implementation: e.g., if your amplifier has a pole-zero doublet, demonstrate why it does not affect amplifier settling, do not only rely on SPICE output.
- Results and supporting details, including figures illustrating the performance and any analytical results that help clarify the design tradeoffs or illuminate critical performance issues. The results must include a breakdown of the total power dissipation into individual contributions (e.g. bias network, first gain stage, second gain stage), plots of the amplifier frequency response and step response (for maximum input step size; zoom in on the settling tails), and a graph or table breaking down the total between the main contributors (e.g. input devices, active load, second gain stage, etc.).
  If you choose a class AB design, report both the static power P_s and the dynamic power dissipation P_d for a maximum size input step (averaged over t_s). Report $P=0.7P_s + 0.3P_d$ as the total average power dissipation of the circuit under typical operating conditions. Remember to check the settling time for small amplitudes since class AB amplifiers are not linear.
- A conclusion that briefly comments on why your design is (or perhaps is not) outstanding.

Grading

Your grade will be based on the following criteria (equal weights):

- Report & Presentation: Abstract, introduction, conciseness, clarity, schematics, simulation results, references, conclusions.
- Approach: How practical is your design? Would it likely work if it was built? Have you addressed potential problems? Analyzed circuit requirements (e.g. bandwidth, gain, matching requirements, safety margins)? Investigated issues not or not well modeled in SPICE (e.g. mismatch of critical devices)?
- Realization: What are the main reasons for your choice of amplifier topology and circuit blocks? Have you correctly modeled and simulated the key aspects of your design?
- Performance: Have all performance specifications been met? If not—what are the limitations, and how could they be overcome? What is the power dissipation of the circuit?

You may either work alone or in a group of two and submit a joint report.