Josephson Junctions in SPICE 2G5

(20 Dec 1982)

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Introduction

This supplement to the SPICE 2G5 User's Guide describes the Josephson junction model which has been implemented by the Cryoelectronics Group at the University of California at Berkeley. The model is only valid for transient simulations; dc operating point and ac small-signal analyses are not allowed.

The following discussion assumes some knowledge of the User's Guide. The last two sections, on implementation of different quasiparticle and control current models and documentation of the device and model linked lists is intended for programmers who have already read *Program Reference for SPICE2*, by Ellis Cohen (ERL Memorandum M592).

Use of .OPTIONS

There are several options which must usually be changed when simulating Josephson circuits. In order to integrate accurately the phase of each junction, fairly small time steps must be used. For a given allowed error, as specified by the option RELTOL, the maximum time step is limited so the maximum phase change is also limited. The default value of RELTOL is 0.001, but most circuits can be accurately simulated with RELTOL = 0.01. Because the limit on phase change is proportional to SQRT(RELTOL), the cost for a simulation is reduced by about a factor of three by using RELTOL=0.01 instead of the default value.

To be able to follow the Josephson oscillations, it is necessary to have a plot interval of less than a picosecond. For example, if 2 mV is expected across a junction and five points per cycle are sufficient, the time interval between output data points should be 0.2 ps. This resolution will usually require a resetting of the LIMPTS option, which limits the total number of output data points and has a default value of 101. If the magnitude of the oscillations is large, a coarse output interval can lead to erroneous results due to sampling aliasing of the oscillations.

Because of the limited time step size, Josephson circuits tend to require a large number of transient analysis iterations. The default limit on the total number of such iterations is 5000. This can be reset by the option ITL5. Example .TRAN and .OPTIONS cards are:

.TRAN 0.2PS 1NSEC UIC

This work was supported by the Office of Naval Research under contract number N00014-77-C-0419.

.OPTIONS LIMPTS=5001 RELTOL=0.01 ITL5=30000

The transient simulation will run for 1 nanosecond with 0.2 picoseconds between outputs. There will be 5001 output points, which will require about 30000 iterations to calculate. The circuit solution must converge to within 0.01 at each time step. Note that UIC (Use Initial Conditions) is specified on the .TRAN card. When Josephson junctions are present, the user must specify the initial conditions for transient simulations. If none is specified on the device card, an initial value of 0 is used for both junction voltage and phase. If the user fails to specify UIC on the .TRAN card, and Josephson junctions are in the circuit, the program will issue a warning and initial conditions will be used.

The user will probably wish to specify other options as well, such as the maximum CPU time allowed. Refer to the User's Guide section on the .OPTIONS card.

Josephson Junctions

General form:

BXXXXXXX N1 N2 NC1 NC2 NPHI MNAME <AREA> <IC=VJ,PHI>

Examples:

B2JN 1 7 8 3 24 JJMOD1 IC=0,3.1416 BINPUT 3 4 2 1 99 NIOB4 AREA=3.0 IC=0.1MV,0.5RADIANS

See Fig. 1 for a schematic of the device. N1 and N2 are the actual device nodes. NC1 and NC2 sense control current.¹ They are connected by the equivalent of a voltage source of zero volts and any current flowing through the source modifies the Josephson current according to the model parameters CCT and ICON described below. NPHI is the phase node. No physical element may be connected to it. MNAME is the model name. AREA is the area factor which multiplies device critical current, quasi-particle conductance, and capacitance. Initial conditions (junction voltage and phase) should always be specified. The phase is measured in radians, but it is treated internally in SPICE as a voltage at NPHI.

Josephson Junction Model

General form:

.MODEL MNAME JJ(<PARAMETER=VALUE>,...)

Examples:

.MODEL JJMOD1 JJ(VG=2.7MV, CAP=0.6PF, RTYPE=2, R0=300HMS, + RN=20HMS, ICRIT=0.8MA) .MODEL NIOB4 JJ(VG=3.8MV, RTYPE=1, CAP=2.0PF, ICRIT=1MA)

See addendum.

name	parameter	default	minimum	maximum	example	area
RTYPE	quasiparticle model	0	0	5	2	
CCT	control current type	0	0	5	1	
VG	gap voltage	2.7mV	1mV	5mV	2.7mV	
DELV	gap transition voltage	0.3mV	$1 \mu V$	½VG	0.1mV	
ICON	control current scale	0.1mA	1μA	1A	1mA	
R0	subgap resistance	200Ω	0	$1M\Omega$	70Ω	*
RN	high voltage resistance	20Ω	0	1kΩ	4Ω	*
ICRIT	critical current	0.1mA	1μA	0.1A	0.4mA	*
CAP	junction capacitance	0	0	100pF	1pF	*
FP1						
to	not used	0	0	1		
FP5						

The model parameters are listed in the table below.

RTYPE selects one of the three types of quasiparticle resistance. A value of 0 gives zero quasiparticle conductance. This is convenient for modeling heavily shunted junctions. A value of 1 gives a piecewise-linear model, as defined in Fig. 2. A value of 2 gives a smoothed resistance model, which uses a Fermi-like function for weighting between R0 and RN:

$$I(V) = V \frac{G_0 + G_n \exp(\gamma)}{1 + \exp(\gamma)}$$
$$\gamma = (|V| - V_{gap})/DELV$$
$$G_0 = 1/R_0; \quad G_n = 1/R_n$$

The transition region is about six times the value of DELV as shown in Fig. 3.

The Josephson current is given by $I_J = I_M(I_{CTL}) * \sin(\phi)$, where I_M is a function specified by the model parameter CCT, I_{CTL} is the current flowing between the control nodes NC1 and NC2, and $\phi = (2e/h) \int V_J dt$. For CCT = 1 or 2, ICON is the value of I_{CTL} for which I_J first goes to zero.

CCT Function

$$\begin{array}{ll} 0 & I_M = ICRIT \\ 1 & I_M = ICRIT * \sin(x)/x \\ & \text{where } x = \pi * I_{CTL}/ICON \\ 2 & I_M = ICRIT * (1 - I_{CTL}/ICON) \text{ for } |I_{CTL}| \leq ICON \\ & I_M = 0 \text{ otherwise} \end{array}$$

Example Josephson Circuit

Listed below is an example input deck which simulates the operation of a Josephson latch. A simplified schematic is in Fig. 4 and a plot of the voltage at node 12 is in Fig. 5.

SELF GATING AND CIRCUIT *SGA REPORTED BY A. DAVIDSON. SIMULATED BY INTERFEROMETERS *WITH FEED INDUCTORS. MODELED BY S. H. DHONG. *CIRCUIT DESCRIPTION VSUP 1 0 PWL(0 0 10PS 0 110PS 10MV 500PS 10MV) IANA 0 5 PWL(0 0 10PS 0.00MA 500PS 0.00MA) IDC 0 8 PWL(0 0 10PS 0.125MA 500PS 0.125MA) X10 3 4 5 6 7 ITFRI3 X30 15 16 13 0 0 ITFRI3 X20 11 12 8 9 13 ITFRI3 X40 18 19 7 0 0 ITFRI3 RF1 1 2 30.250HMS RA1232OHMS RA22420HMS **RF3 4 14 30HMS** RB1 14 15 20HMS RB2 14 16 20HMS RC1 10 11 20HMS RC2 10 12 20HMS RTER29060HMS RTER16060HMS RF4 12 17 30HMS RD1 17 18 20HMS RD2 17 19 20HMS RTOUT 16 0 30HMS RCOUT 19 0 30HMS RQ1 1 10 30.250HMS SUBCKT ITFRI3 1 2 3 4 5 *A THREE-JUNCTION INTERFEROMETER WITH 5MICRON DESIGN RULES *INPUT NODES ARE 1 AND 2. CONTROL NODES ARE 3 AND 4. NODE 5 IS *THE CURRENT RETURN NODE. B1 9 15 100 0 101 JJMOD1 IC=0,0 B2 13 5 102 0 103 JJMOD1 IC=0,0 AREA=2.0 B3 11 16 104 0 105 JJMOD1 IC=0,0 RDUM5 100 0 1 RDUM6 102 0 1 RDUM7 104 0 1 LC1 3 6 19PH LC2 6 7 19PH LC3 7 8 19PH LC48419PH CC1 3 0 0.2PF CC2 6 0 0.2PF CC3 7 0 0.2PF CC4 8 0 0.2PF CC5900.2PF L1912.52PH L2 1 10 3.37PH

L3 10 2 3.37PH L4 2 11 2.52PH L5 15 5 1.0PH L6 5 16 1.0PH LD1 9 12 0.8PH LD2 10 14 0.8PH RD1 12 10 2.00HMS RD2 14 11 2.00HMS LS 10 13 0.06PH CG2 1 0 0.7PF CG4 2 0 0.7PF K1 LC1 L1 0.303 K2 LC2 L2 0.337 K3 LC3 L3 0.337 K4 LC4 L4 0.303 .ENDS ITFRI3 .MODEL JJMOD1 JJ(VG=2.5MV,CAP=0.78PF,RTYPE=1,DELV=0.6MV, +CCT=0,ICRIT=0.1MA,R0=200.0OHMS,RN=26.2OHMS) .TRAN 1PS 300PS UIC .OPTIONS ACCT LIMPTS=1000 ITL5=10000 RELTOL=0.005 .PRINT TRAN V(16) V(19) V(4) V(12) .PLOT TRAN V(16) V(19) V(4) V(12)(-3MV,3MV) .END

Implementation of Other Models

It is possible for the user to implement other models of quasiparticle resistance and control current characteristics. To implement CCT = 3, 4, or 5, the user must write a corresponding FORTRAN function UJJCT3, UJJCT4, or UJJCT5, and replace the corresponding dummy function in the source code. The function should return a critical current multiplier as a function of I_{CTL} and ICON. The functions are called from subroutine JOJUNC.

The user may also implement UJJCF3, 4, or 5 which correspond to RTYPE = 3, 4, and 5. These subroutines return the DC quasiparticle current and the incremental quasiparticle conductance. See subroutine JOJUNC for the order of input and output parameters.

To allow implementation of additional model parameters for any functions and subroutines, model parameters FP1 through FP5 have been set aside. These may be specified on the .MODEL card and are then accessible to the corresponding devices. These parameters are presently limited to values between 0 and 1 by subroutine MODCHK.

Linked List Specifications

Listed below are the linked lists for Josephson junctions. The device and model linked lists are discussed in Section 13 of *Program Reference for SPICE2*, by Ellis Cohen.

Josephson junction devices:

Name: BXXXXXXX

ID: 18

Linked list:

LOC+0 next pointer

-1 subckt info

+1 LOCV +2 nd1 (device node 1) +3 nd2 (device node 2) +4 nc1 (control node 1) +5 nc2 (control node 2) +6 nint (phase integration node) +7 mp (model pointer) +8 off (not used yet) +9 (nd1,nd2) +10 (nd2,nd1)+11 (nd1,nd1) +12 (nd2,nd2)+13 (nint,nint) +14 IBR +15 (nc1,IBR) +16 (nc2,IBR) +17 (IBR,nc1) +18 (IBR,nc2) +19 LXi offset +20 LD offset +21 (nint,nd1) +22 (nint,nd2)

	+23.
	. reserved, not yet used
	+28.
LOCV+0 element name	
	+1 area factor
	+2 IC: voltage across device
	+3 IC: voltage on nint == phase angle
LXi+0 vj0	1 0
	+1 cs0
	+2 gq0
	+3 cq0
	+4 pino
	+5 qj0 +6 cai0
	+7 aphi
	+8 caphi
	+9 crt0
	+10 extra place
	+11 extra place
Josephson model	
Josephson model	
	Model type: JJ
	ID: 25
T • 1 • 1 • .	
Linked list:	
LOC 10 next pointer	-1 SUDCKI INIO
LOC+0 liext politier	+1 LOCV
	+2 polarity (always = 0)
LOCV+0 model name	model card names:
	+1 resistance typeRTYPE
	+2 control current type CCT
	+3 gap voltageVG
	+4 VsubT, delta VDELV
	+5 Icon sensitivityICON
	+6 low voltage conductanceR0
	+/ normal conductanceKN
	$+\delta$ maximum critical currentiCKII
	+> capacitanceCAP
	+11 "FP?
	+12 "FP3
	+13 "FP4
	+14 "FP5

Fig. 1. Josephson junction model schematic.

- Fig. 2. PWL resistance model.
- Fig. 3. Smoothed resistance model.
- Fig. 4. Simplified schematic of latch.
- Fig. 5. Voltage waveform at node 12.