Behavioral Representations for VCO and Detectors in Phase-Lock Systems

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Abstract

This paper presents behavioral representations for detectors and voltage-controlled oscillators that are independent of circuit architectures. Parameter extraction techniques are described. Finally, parameter extraction for a VCO is demonstrated, and an example PLL constructed using the models is simulated and verified against actual chip measurements.

1 Introduction

Behavioral simulation is used in our constraint-driven, top-down hierarchical design methodology[1] to verify the design early. In digital domain, the behavior of a circuit is defined to be the function to be implemented independent of the architecture and/or schematics. Behavioral simulation in digital circuits can reduce substantially the design cycle. In the analog domain, behavioral simulation is often confused with macromodeling where an approximate model is built with components that are typical circuit components such as capacitors, controlled sources, and resistors. The notion of behavior as given for digital circuits could be extended to the analog domain. However, since the high-level analog functions are very simple, the power of behavioral simulation to uncover potential problems is greatly reduced. In analog circuits, malfunctioning is mostly due to the non-ideal behavior of the components. Thus, an effective behavioral simulation strategy has to be based on high-level models of *second order effects*. We have developed models for A/D converters that are based on these principles[2][3][4]. To have a useful behavioral simulation environment, we need to develop models for most of the high-level analog functions. In this paper, we propose behavioral representations for voltage-controlled oscillators (VCO) and detectors that are essential circuit components in any phase-lock system. The representations include sufficient second order effects for realism, are *independent* of the circuit component architectures, and are general for use in many diverse phase-lock system modeling applications. The paper is organized as follows: Behavioral models for sinusoidal and square wave VCO's are presented in Section 2 and 3, respectively. In Section 2.3, results of parameter extraction for a VCO are compared with SPICE and macromodeling results. A behavioral model for detectors and parameter extraction techniques are presented in Section 4. Finally, in Section 5, a phase-locked loop application is presented with simulation results compared with actual measurements.

2 Sinusoidal VCO

A sinusoidal voltage-controlled oscillator (VCO) ideally accepts as input a voltage, v, and outputs a sinusoidal signal whose frequency is linearly proportional to the input voltage. In a practical VCO, the frequency is nonlinearly related to the input voltage, the output contains harmonic components (distortion), and the phase has random variations (phase noise). Previous work[5] [6] includes macromodels for SPICE which do not model distortion or noise effects. In our model, non-ideal behaviors can be captured by a two stage model shown in Figure 1, where stage

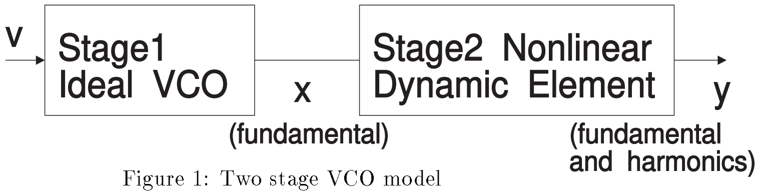

Figure 1: Two stage VCO model

1 is an ideal VCO to generate a signal, x, followed by a nonlinear dynamic stage 2 whose output, y, contains fundamental and harmonic frequencies. Given the input v, the output of stage 1, x, is given by

$$f = g(v) \tag{1}$$

$$\Phi(t) = 2\pi \int_0^t f(\tau)d\tau + \Psi(t) \tag{2}$$

$$x(t) = cos(\Phi(t)) \tag{3}$$

where g is the nonlinear relationship between the frequency f and v, Φ is the instantaneous phase, and Ψ is any stationary random process to represent phase noise (usually Gaussian with mean ψ_0 and variance σ^2). Since f and Ψ are in general time-varying, x is not sinusoidal. When such a signal is fed into the nonlinear dynamic stage 2, the output y is given by

$$y = \sum_{n=1}^{\infty} \int \cdots \int h_n(\tau_1, \ldots, \tau_n)x(t-\tau_1)\ldots x(t-\tau_n)d\tau_1 \ldots d\tau_n \tag{4}$$

where h_n are the Volterra kernels[7] of stage 2. To solve (4), we make the **quasi-static** approximation.

2.1 Quasi-static approximation

In a practical sinusoidal VCO, the phase noise Ψ is small, the control range is small, and the control voltage varies much slowlier than the frequency f. Therefore, we propose to determine VCO model parameters for a range of *constant* values of v using (4). The quasi-static approximation means that *during simulation for time-varying $v(t)$, we use the model parameters corresponding to instantaneous values of v.* If v is a constant, then x is a pure sinusoidal, and (4) has solution,

$$y = \sum_{n=0}^{N} |A_n(\omega)| cos(n\Phi(t) + \angle A_n(\omega)) \tag{5}$$

where N is the order of approximation, $\omega = \frac{d\Phi}{dt}$ is the constant frequency, and A_n are complex coefficients given by

$$A_0(\omega) = \frac{1}{2}H_2(\omega,-\omega)e^{j\Psi}, A_1(\omega) = (H_1(\omega)+\frac{3}{4}H_3(\omega,\omega,-\omega))e^{j\Psi},$$

$$A_2(\omega) = \frac{1}{2}H_2(\omega,\omega)e^{j\Psi}, A_3(\omega) = \frac{1}{4}H_3(\omega,\omega,\omega)e^{j\Psi}, etc$$

Summarizing, the VCO model consists of stage 1 described by (1), (2), and (3), and stage 2 described by (5). The model parameters are the function g, the phase noise Ψ, and the complex coefficients A_n.

2.2 VCO parameter extraction

Parameters g, Ψ, and coefficients A_n can be estimated from VCO outputs $y(t,v)$ for different fixed values of v obtained from SPICE simulations or laboratory measurements. The following steps are followed: (a) For a constant input v, estimate from output y the fundamental frequency, f, using the sinusoidal minimum error method[8] or the complex demodulation method[9]. In the latter case, the idea is to multiply $y(t,v)$ with $e^{j2\pi\hat{f}t}$, followed by low pass filtering to get $z(t)$, where $\hat{f}$ is our guess of f. If $\hat{f} = f$, the phase of $z(t)$ is constant; otherwise, it is slowly time-varying for $\hat{f} \approx f$. Using Newton-Raphson[10], solve for f such that the phase of $z(t)$ is constant. (b) With f known, the magnitude and phase of the fundamental and harmonics can be similarly calculated using demodulation. Specifically, magnitude is the average of $2|z(t)|$ and phase is the average of $-\angle z(t)$. (c) Repeat (a) and (b) for different v to estimate the nonlinear function g for equation (1), as well as for more data points on $A_n(\omega)$ in (5). (d) Estimate σ for (2) from laboratory measurements or by hand analysis[11]. (Notice that SPICE does not simulate noise in the time domain.) (e) Assign value for ψ_0, which is the only initial condition.

2.3 Example VCO parameter extraction

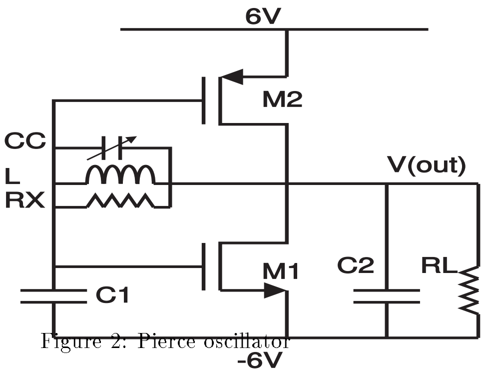

Figure 2: Pierce oscillator

Shown in Figure 2 is a schematic of a Pierce oscillator with varactor tuning that consists of circuit elements $M1 = 15\mu m/1\mu m$, $M2 = 35\mu m/1\mu m$, $L = 129.75nH$, $C1 = C2 = 20pF$, $RL = 100\Omega$, $RX = 1M\Omega$, and voltage-controlled capacitor $CC = 2pF/V$. Its behavioral model parameters (Figure 3) were extracted from three SPICE transient simulations for three different control voltage v. Figure 4 shows the SPICE output for $v = 0$ and the residual error in the 5^{th} order (N=5) behavioral approximation used in this case. In contrast, the SPICE

v	0	1	2
n	(gain,phase)	(gain,phase)	(gain,phase)
1	(2.88V, -3.72)	(2.88V, -4.10)	(2.88V, -4.47)
2	(1.63mV, -0.89)	(2.00mV, -1.29)	(2.02mV, -1.77)
3	(78.2mV, -3.02)	(78.0mV, -4.17)	(78.2mV, -5.27)
4	(30.2μ V, -1.90)	(45.6μ V, -0.92)	(36.3μ V,-1.08)
5	(6.65mV, -1.37)	(6.63mV, -3.29)	(6.69mV, -5.12)

Figure 3: Behavioral parameters for Pierce oscillator

macromodels in [5] do not model harmonics, so the lower error bound is given by the first order residual error shown in Figure 5. Thus, the behavioral model is *more accurate* than macromodels, as well as *faster* since evaluating the behavioral model only involves evaluating the function in (5).

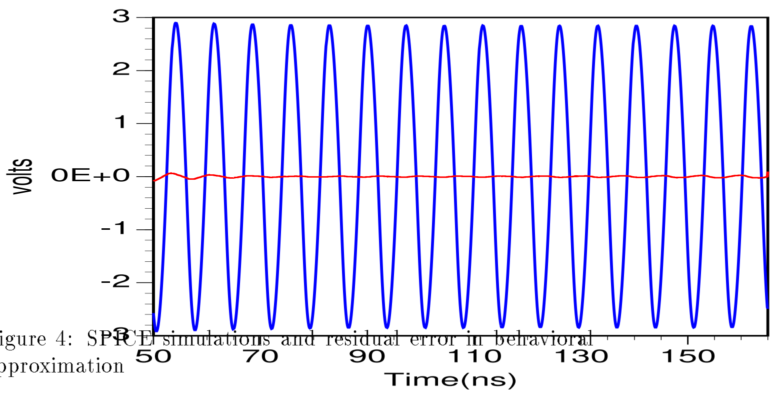

Figure 4: SPICE simulations and residual error in behavioral approximation

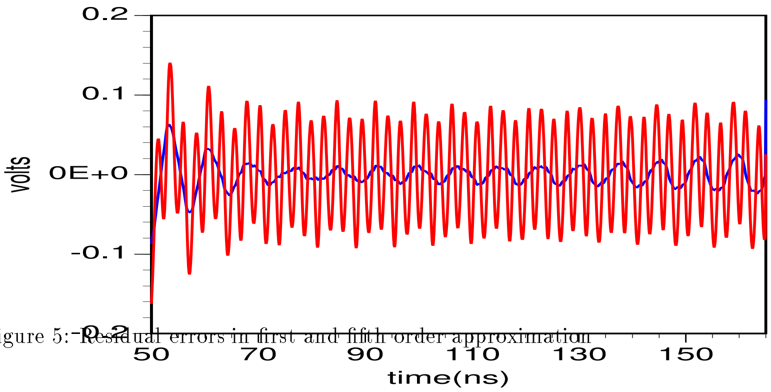

Figure 5: Residual errors in first and fifth order approximation

2.4 Error analysis

To estimate the error of the quasi-static approximation when the control input is not constant, we let the frequency, f, be modulated by a sinusoidal signal with small amplitude (narrow band frequency modulation). For instance,

$$f = g(v) = f_c + \beta f_m cos(2\pi f_m t)$$

where β is the modulation index, and f_m is the modulation frequency. Assuming the phase noise is negligible, it can be shown that the error of the quasi-static approximation is bounded by an error term proportional to β. As a result, when the modulation index β is sufficiently small, the error becomes negligible.

3 Square wave VCO

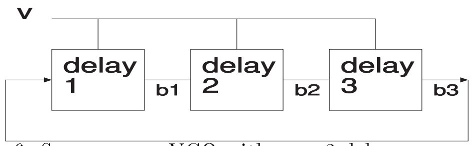

Figure 6: Square wave VCO with $m = 3$ delays

In addition to oscillators with sinusoidal outputs, there are oscillators with square wave outputs. In contrast to the sinusoidal VCO where the waveform is represented by (5), the waveform of a square wave is represented by the zero crossings (low-to-high and high-to-low transition times). In general, a VCO consists of m delay elements connected in a ring structure (Figure 6). Each of the m outputs are phased shifted by $\frac{1}{2mf}$ seconds, where f is the frequency of the VCO. We represent the j^{th} transition time of output i with $y_i(j)$ as shown in Figure 7. Similar to

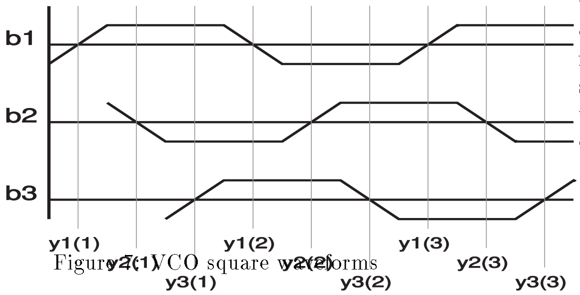

Figure 7: VCO square waveforms

the sinusoidal VCO, the frequency is controlled by the input v using equation

$$f_i = g_i(v) \quad (6)$$

where g_i represents control relationship for element i, and f_i represents the effective frequency of delay element i. Unfortunately, v varies considerably in a square wave VCO; therefore, the quasi-static approximation is not appropriate in this case. The transition times are determined by the delay between adjacent delay elements. For example, $y_i(j)$ for $i \neq 1$ is equal to $y_{i-1}(j)$ plus the delay of element i. Because of this relationship, it is convenient to use a recursive definition for $y_i(j)$,

$$\pi = 2\pi m \int_{y_{i-1}(j)}^{y_i(j)} f_i(\tau)d\tau + \Psi_i(y_i(j)) - \Psi_i(y_{i-1}(j)), i \neq 1 \quad (7)$$

$$\pi = 2\pi m \int_{y_m(j-1)}^{y_i(j)} f_i(\tau)d\tau + \Psi_i(y_i(j)) - \Psi_i(y_m(j-1)), i = 1 \quad (8)$$

where Ψ_i is the random phase noise of element i. Summarizing, the model consists of (6), (7), and (8). Model parameters are the number of delay elements m, the voltage-control relationship g_i, the phase noise Ψ_i, and the initial condition $y_1(1)$.

4 Detectors

A detector compares two signals (input waveform and VCO waveform). Traditionally, circuit designers represent a detector by its phase characteristic which plots the average product of the input waveform and the VCO waveform as a function of the phase difference between the two waveforms. One problem with this modeling approach is that the phase characteristic is defined only when the input waveform and the VCO waveform have the same frequency. As a result, this approach cannot be used during phase-locked loop acquisition. Another problem is that the phase characteristic depends on the shape of the waveforms, so the characteristic is not defined until input signals are applied. As a result, the phase characteristic is not appropriate as a behavioral representation.

Detectors are classified into two broad categories[12]: multipliers (zero memory circuits) and sequential circuits (with memory). In this paper, sequential circuits are represented by state machines with analog inputs, a and b, analog outputs $g(a, b)$, and clock triggered by zero crossings of a and b. Moreover, the same representation can be used for multipliers if they are considered as state machines with a single state and no clock. In general, all detectors can be conveniently represented by a state transition table such as the one shown in Figure 8 for a phase-frequency detector. Signals a, b, and c are the input, VCO, and output waveforms, respectively. The first column is the state number; the second column is the next state if a crosses zero; the third column is the next state if b crosses zero; t_d are gate delays of next state logic; the last column is the output $g(a, b)$ for each state. State transition tables for common detectors are shown in Figure 9. Since all known detectors can be written in this representation, this representation is general and independent of the circuit architecture.

state	a crosses (next, delay)	b crosses (next, delay)	c g(a,b)
0	(1, t_d)	(2, t_d)	0.0
1	(1, t_d)	(0, t_d)	Iup
2	(0, t_d)	(2, t_d)	Idown

Figure 8: Behavioral model for phase frequency detector

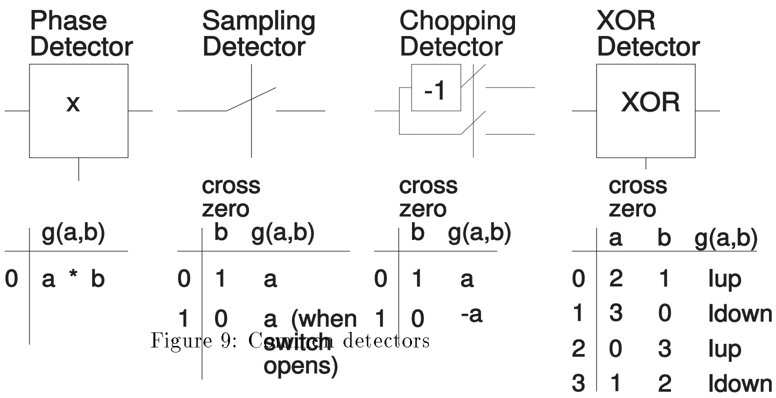

Figure 9: Common detectors

4.1 Detector parameter extraction

For a given detector type, the next state logic is fixed. Nonidealities are the transition delays, t_d, and deviations of the output function. t_d is computed by measuring the total gate delays in the next state logic. Typically, $g(a, b)$ is very simple; for instance, $g(a, b) = c_0 + c_1 a + c_2 b + c_3 ab$. Its non-idealities include constant offset error in c_0 and multiplier gain error in c_3. All four coefficients $c_0 \ldots c_3$ can be extracted using four DC SPICE simulations with different $a's$ and $b's$, and solving for the coefficients in a system of four equations.

5 Phase-lock loop simulation

Using the models presented, we constructed a high-level model of a real phase-lock loop[13]. The loop filters are modeled with differential equations, the VCO is modeled with a square wave VCO with one delay element ($m = 1$, output fed directly back to input), and the phase-frequency detector is modeled as in Figure 8 with $t_d = 0$. Relevant system parameters, such as acquisition time and jitter gain function, are computed from transient simulations. In our prototype, the VCO output, b, is modeled as a switching function, which is completely characterized by the transition points, $y_1(j)$. Traditional integration algorithm for differential equations cannot handle this type of system because b is non-differentiable. However, the problem is much easier because the differential equation solver needs only determine the transition time points, $y_1(j)$, which are defined by (8). For example, in (8), we need to find the upper integration limit, $y_1(j)$, to satisfy the equation. As a result, *we solve for $y_1(j)$ by using an iterative solver on top of an integration algorithm.* For prototyping, we implemented the iterative false position method[10] on top of the trapezoidal integration algorithm to search for the points. Using this algorithm, the simulation speed is dramatically increased, while preserving numerical stability.

A prototype simulator has been implemented using the C++ language on a DECstation 5000. Figure 10 shows the output frequency as the input frequency is stepped from 120MHz to 138.5MHz, compared with the output frequency measured from an experimental chip. From Figure 11, measured overshoot (34%) and settling ($8\mu s$) agree with simulation (33%, $7\mu s$). Next, the input frequency is varied to probe the system for the jitter gain function. From the data, -3db cross-over frequency is estimated to be 470KHz which agrees with the theoretical value of 410KHz. For both examples, the circuit was simulated from time zero to $40\mu s$ (using DEC5000 CPU time 17 minutes), corresponding to 5165 VCO cycles. If the same analysis is done with SPICE, the time step size should be about $100ps$ since the VCO period is $8.3ns$. So, assuming SPICE takes $0.5s$ to compute a time point, SPICE would take at least 2 days for each of the examples.

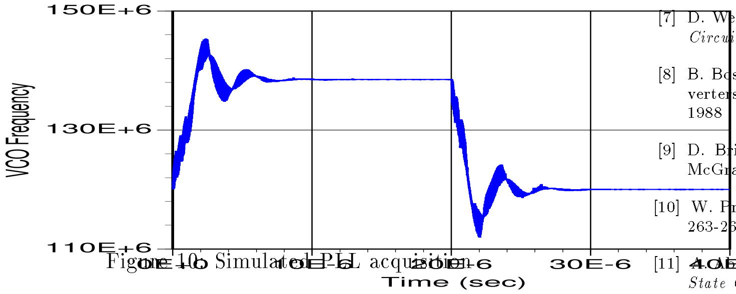

Figure 10: Simulated PLL acquisition

6 Summary

We have presented behavioral models for VCO and detectors in phase-lock systems. Parameter extraction techniques to identify the models have been described, and the techniques were used to extract parameters for an actual VCO. Furthermore, we used these models to model and simulate an actual PLL. The simulation time is significantly lower than an estimated SPICE simulation time, and the simulation results agree with measured chip data. Finally, because our models are independent of circuit architecture, we can model and simulate a wide range of PLL circuits. We have presented a way to model and simulate PLL's in a reasonable amount of time with minimal loss of accuracy.

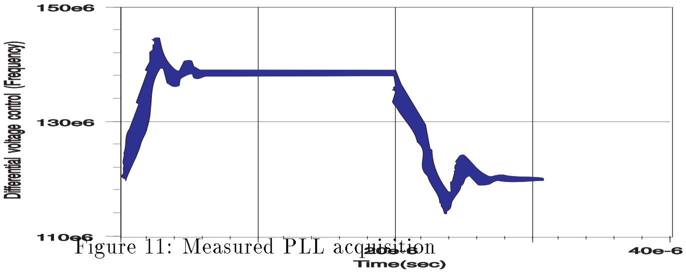

Figure 11: Measured PLL acquisition

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