A Performance-Driven Router for RF and Microwave Analog Circuit Design

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Abstract

Techniques are proposed for the routing of very high-frequency circuits. In this approach, performance sensitivities are used to derive a set of bounds on critical parasitics and to generate weights for a cost function which drives an area router. In addition to these bounds, design often requires that the length of interconnect lines be equal to predefined values. The routing scheme enforces both types of constraints in two phases. During the first phase all parasitic constraints are enforced on all nets. Equality constraints are enforced during the second phase by expanding each net simultaneously while ensuring that no additional violations to parasitic constraints are introduced in the layout. During both phases accurate and efficient parasitic estimations are guaranteed by compact analytical models, based on 2-D and 3-D field analysis. Finally, a global check on all distributed parasitics is performed. If the original constraints are not satisfied, the weights are updated based on severity of the violation and routing is applied iteratively. Several layouts synthesized using this technique have been fabricated and successfully tested, confirming the effectiveness of the approach.

1 Introduction

Great effort has been devoted over the years to create general purpose CAD tools for schematic design and optimization of RF and microwave circuits, e.g. [1, 2]. Layout synthesis has not received comparable attention in the literature due to the inherent complexity of the problem and to the lack of designs whose size could justify a CAD based approach. More recently however, the increasing complexity of monolithic RF and microwave integrated circuits (MMIC) suggests that an automated approach to the physical synthesis is preferable for efficiency, reliability and yield considerations.

LINMIC [3] and later [1] proposed a knowledge-based interactive approach aimed at designers with minimum expertise by providing aids for low frequencies design of MMICs. However, due to the lack of an explicit reference to performance, the synthesis process could result in a large number of time-consuming iterations necessary to satisfy specifications.

Other semi-automated topology-driven approaches to the routing of MMICs have also been proposed [4, 5]. These systems include template-based routines for the abutment of pre-defined cells implementing devices as well as interconnect. The knowledge of the relative position of all cells provides the starting point of the layout realization, thus strongly limiting the flexibility of the approach and its applicability to complex designs.

We propose a constraint-based approach to the layout synthesis of MMICs. In this paper we focus on the routing problem. The flow diagram of the approach is shown in Figure 1. Firstly, high-frequency performance specifications are mapped onto a set of bounds on all classes of distributed parasitics. Then, using sensitivity analysis, a set of weights is calculated for the area router. The role of the weights is to control a cost function which penalizes those realizations with highly critical parasitics. Layout synthesis of RF an microwave circuits almost always requires that the dimensions of some interconnect lines be fixed. However, length constraints on interconnect cannot be effectively enforced during this phase. Hence, the routing or *constructive phase* is followed by by a *refinement phase*. The refinement consists on progressive expansion of all nets simultaneously thus allowing enforcement of all net constraints while no new violations are created on the remaining parasitic constraints. If infeasibility is detected a new set of weights is generated and the cycle is repeated. At the completion of the layout, the entire circuit is checked against constraint violations so as to verify that all performance specifications are met. Parasitics are directly extracted from all physical geometries and estimated by means of *ad hoc* analytical models based on 2-D and 3-D field analysis. In case a specification violation occurs, the parasitics responsible for the violation are identified and a sensitivity-based scheme is used to create a new set of weights. The cycle is then restarted. The finite step loop ends when all specifications are met.

There are several advantages to this approach. A constraint-based approach to the layout of RF and microwave circuits helps drastically reduce the number design iterations by carefully modeling and controlling all relevant parasitic effects in the circuit. For a given technology, compact and accurate models for physical parasitics are derived only once. Hence the synthesis and analysis of a circuit is efficient and can be effectively used within a larger semi- or fully automated design cycle. Furthermore, using a different cost weighting scheme, rapid circuit redesign for different realization and performance requirements can be efficiently accomplished. This is particularly useful in the design of large scale MMIC libraries.

The paper is organized as follows. In Section 2 the models for interconnect used in our layout synthesis approach are presented and the process of generating constraints on layout components is described. In Section 3 the constructive and the refinement phases of the router are outlined and in Section 4 the practical suitability of the approach is demonstrated through an example.

2 Parasitic Modeling and Constraint Generation

Accurate interconnect modeling is a fundamental requirement of a constraint-driven approach to the routing of RF and microwave circuits. For reasons of efficiency closed formulae and analytical models for interconnect lines and all relevant parasitics are desirable. Since the area of application of this work is MMICs, all interconnect lines are modeled as microstrip transmission lines. Parasitic effects such as inductive and capacitive crosstalk are modeled im terms of the degradation induced on the characteristic impedance Z_o and loss α. Alternatively at low frequencies discrete (R,C,L) parasitics can be used. Analytical models of all considered parasitics are obtained by fitting appropriate mathematical expressions to data obtained from 2-D or 3-D field solvers as proposed by [6].

Interconnect discontinuities are modeled using discrete components, while radiation and surface-wave propagation effects have been neglected due to

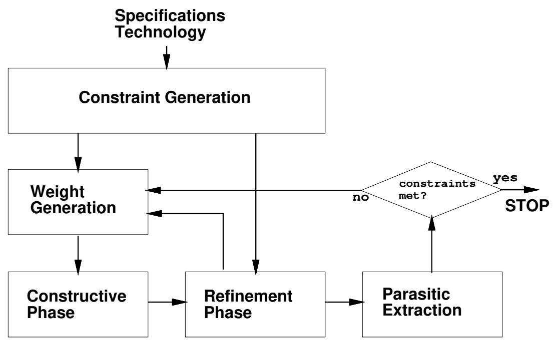
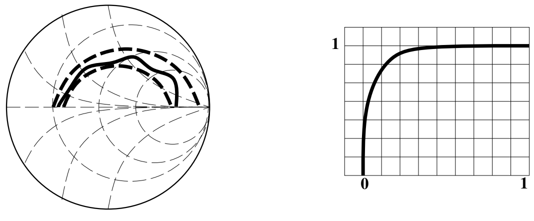


Figure 1*: Flow diagram of the tool.*



(a) (b)

Figure 2: *(a) Microwave specification. (b) Cost function for constrained optimization.*

the the relative small circuit size if compared with the signal wavelengths [7]. If needed, surface-wave propagation could easily be modeled using the closed forms reported in [8]. Substrate-dependent losses have been taken into account in the full model. A summary of the formulae used in our approach for estimating Z_o and α can be found in [9].

The constraint generation techniques outlined in [10] and [11] need be modified to account for the distributed nature of parasitics in microwave circuits. For a given a performance K_i, let us define *performance specification* the set of inequalities which determine lower- and upper-bounds for K_i and the range of frequencies for which they are valid. For example, consider the input reflection coefficient S_{11} illustrated in Figure 2 (a). The solid line is the actual value of S_{11} obtained from the complete layout after extraction and the dotted lines are the frequency dependent specifications to performance S_{11}, or

$$
\begin{aligned}
&|L_0| \le |S_{11}| \le |U_0|,\ \angle L_0 \le \angle S_{11} \le \angle U_0,\ for\ f_0 - \triangle f_0 \le f \le f_0 + \triangle f_0 \\
&|L_1| \le |S_{11}| \le |U_1|,\ \angle L_1 \le \angle S_{11} \le \angle U_1,\ for\ f_1 - \triangle f_1 \le f \le f_1 + \triangle f_1 \\
&\ldots \\
&|L_n| \le |S_{11}| \le |U_n|,\ \angle L_n \le \angle S_{11} \le \angle U_n, \\
&\qquad\qquad\qquad\qquad for\ f_n - \triangle f_n \le f \le f_n + \triangle f_n\ .
\end{aligned}
$$

In general, for a set of performances $\{K_i\},\ i = 1, ..., N_w$ and a set of parasitics $\{p_j\},\ j = 1, ..., N_p$, *parasitic constraint generation* is defined as the process of creating an inequality constraint on a subset of all parasitics $\{p_j\}$: $p_j \le p_j^{(bound)}$, to guarantee the fulfillment of all performance constraints in the entire frequency range or $\triangle K_i(f) \le \overline{\triangle K_i(f)},\ \forall i = 1, \ldots, N_w, \forall f \in [f_{min}, f_{max}]$. $\triangle K_i(f)$ represents the total and $\overline{\triangle K_i(f)}$ the maximum allowed degradation of performance K_i with respect to all parasitics within the entire range of operation. Parasitics such as cross-couplings, characteristic impedance degradation, losses and microstrip line length tolerances are constrained in this fashion. Constraints on parasitics related to short and open microtrip terminations are derived from the above constraints as described in [9].

Assuming that performance is linear near its nominal value at all frequencies, it can be represented as a linear combination of its sensitivity with respect to all distributed parasitics at all frequencies. Since parasitics can contribute constructively as well as destructively to performance, positive and negative sensitivities must be considered separately for constraint computation. Positive and negative components of the performance degradation $\triangle K_i^+$ and $\triangle K_i^-$ with respect to all parasitics belonging to the set $\{p_j\}$ are, in first approximation

$$
\triangle K_i(f)^+ = \sum_j S_j^i(f)^+\ p_j\ ,\quad \triangle K_i(f)^- = \sum_j S_j^i(f)^-\ p_j \qquad (1)
$$

Technology-related process variations can be taken into account by replacing nominal values of sensitivities with worst-case values [10] or by finding bounds on parasitic and device mismatches [11].

To insure that all relevant parasitics are considered during the optimization, each interconnect line to be implemented in the circuit is modeled as a microstrip line with inductive and capacitive coupling with all the other nets. A numerical sensitivity analysis is performed for each performance function using simulator MNS [4]. All parasitics, whose cumulative contribution to performance degradation is negligible, are automatically discarded. Bounds on critical distributed parasitics are calculated by using constrained optimization, the objective being the maximization of the flexibility of the

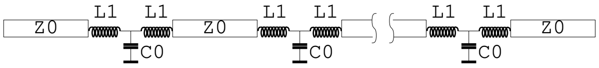


Figure 3: *Interconnect model for microstripline with multiple bends.*

layout generation process. The objective function of the optimizer, PMW , is a polynomial of second order monotonic in the range from zero to one, as shown in Figure 2 (b). The goal is to obtain large bounds on critical parasitics, while at the same unnecessarily loose bounds on uncritical parasitics are allowed to be tightened.

RF and microwave circuits rely for functionality on transmission lines with a specific length. However tolerances $\triangle L_j^{\pm}$ from nominal value L_j should be permitted to provide more flexibility to the router:

$$
\ell_j = L_j\ ,\ \ \triangle \ell_j^+ \le \triangle L_j^+\ ,\ and\ \ \triangle \ell_j^- \le \triangle L_j^-\ ,
$$

While L_j is determined by design, constraints $\triangle L_j^{+/-}$ must be computed numerically. Using MNS the sensitivity of each performance with respect to length variations can be quantified, thus, using constrained optimization, constraints on the tolerances are calculated.

Parasitics involving the detailed realization of interconnect such as bends, gaps and steps need be considered in a somewhat different way. A bended interconnect realization is shown in Figure 3, where the bends have been replaced with appropriate models [9]. Consider the problem of finding a constraint on the number of bends in the microstrip line.

Suppose a microstrip line of nominal length L is partitioned into N segments of length L/N each. Let us model $N-1$ bends as in Figure 3. Due to the repetitive character of the model, performance sensitivities with respect to the discrete components $S_{L/C}^K$ of each bend are necessarily equal. Therefore the cumulative degradation $\triangle K$ of N bends is

$$
\triangle K = \sum_{i=1}^{N-1} (S_{L_1}^K L_1 + S_{C_0}^K C_0) = (N-1)(S_{L_1}^K L_1 + S_{C_0}^K C_0)
$$

Consequently only one (L_1, C_0) pair must considered by the optimizer. After the optimization two scenarios are possible: (a) parasitics are not critical and therefore they have been eliminated. In this case, given the maximum and minimum values for C_0 and L_1, $N^{(bound)}$ can be computed as following

$$
N^{(bound)} = 1 + min\{\lfloor C_0^{(max)}/C_0^{(min)} \rfloor, \lfloor L_1^{(max)}/L_1^{(min)} \rfloor\}
$$

Note that if $C_0^{(min)} = 0$ and $L_1^{(min)} = 0$, the constraint on N is ∞, thus it can be neglected.

(b) parasitics are critical and bounded. In this case $N^{(bound)}$ can be obtained by replacing the maximum value of C_0 and L_1 with its bound.

$$
N^{(bound)} = 1 + min\{\lfloor C_0^{(bound)}/C_0^{(min)} \rfloor, \lfloor L_1^{(bound)}/L_1^{(min)} \rfloor\}
$$

3 Routing

For reasons of flexibility and algorithmic reliability, an area routing scheme has been used in our approach. In this scheme all inequality constraints can be easily implemented in the cost function driving the router. Equality constraints however cannot be handled effectively via a cost function, due to the instability they induce in the algorithm [12, Chp.3]. Thus, the routing scheme has been partitioned into two phases. During the first phase, the *constructive phase*, all inequality constraints, i.e. constraints related to interconnect parasitics, are enforced. The second phase or *refinement*, enforces all equality constraints while no new parasitic violations are introduced. Both phases have been implemented in a tool called CORAL .

The first phase of the routing scheme consists of a maze router based on the A* algorithm [13]. The A* algorithm is based on a heuristic estimation of the cost of a path connecting the propagation node on the grid x and a terminal target. An optimal path for a net j is defined as the path minimizing a cost function $f(x)$. $f(x)$ is the estimate of the wiring length ℓ weighted by a factor proportional to interconnect crowding $K_c(x)$ and to the sum of all violations to parasitic constraints.

$$
\begin{aligned}
f(x) = \ell(x) \Bigg(& 1 + K_c(x) + w_j^R\ \frac{Viol[R_j(x)]}{R^0} + w_j^C\ \frac{Viol[C_j(x)]}{C^0} \\
& + \frac{1}{C^0} \sum_{jk} w_{jk}^C\ Viol[C_{jk}(x)] + w_j^Z\ \frac{Viol[Z_j(x)]}{Z^0} \Bigg)\ ,
\end{aligned}
$$

where

$R_j(x)$ = integral of the estimated transmission line loss of net j at x
$C_j(x)$ = integral of the estimated substrate capacitance of net j at x
$C_{jk}(x)$ = integral of the estimated coupling between nets j and k at x
$Z_j(x)$ = *local* estimated characteristic impedance from nominal for net j at x

Every violation ($Viol$[.]) is calculated as the difference between the estimate of the parasitic component (Section 2) and its pre-computed constraint, when this value is positive, otherwise it is set to zero. Parameters R^0, C^0 and Z^0 are normalization factors. w_j^R, w_j^C, w_{jk}^C and w_j^Z are specific weights, calculated according to the equation

$$w_j^{\cdot} = w_0 \sum_{i,f} \left[\frac{S_j^i(f)^-}{\overline{\triangle K_i(f)^-}} + \frac{S_j^i(f)^+}{\overline{\triangle K_i(f)^+}} \right]$$

where $\overline{\triangle K_i(f)^{+/-}}$ represents the specification of performance K_i at frequency f, $S_j^i(f)^{+/-}$ its sensitivity with respect to parasitic p_j and w_0 a normalization factor.

The constructive phase yields interconnects with a minimized length ℓ. Since ℓ cannot be further reduced, the algorithm stops if loss and substrate capacitance violations occur or if the maximum transmission line length L is exceeded. This technique can also be used for implementing stubs simply by creating a virtual target in an area where no parasitic violations can occur [9]. The routing order of the nets is determined automatically giving priority to the wiring of stubs and of nets on which parasitic constraints are tightest. This is done to not compromise the ability of the router to meet all parasitic constraints by routing first non-critical nets.

The refinement phase is responsible for the enforcement of all equality constraints while insuring that no additional violation be introduced in the layout. Refinement is only applied to the set of all nets for which at least a violation exists, call C such set. Consider the constraint on microstripline length of net j, L_j. Since previously obtained length is guaranteed to be smaller than the constraint, the interconnect needs be expanded. However the expansion must occur inside a space where no constraint violations are possible. Call this space *feasibility zone* of net j, or $\mathcal{F}_j$. $\mathcal{F}_j$ is defined as the intersection of all spaces $\mathcal{B}_j(p_k)$, for which parasitic p_k associated with net j does not exceed its predefined constraint.

Assume that each parasitic can be expressed in form of a n^{th} order polynomial $\mathcal{P}_n(\mathbf{x}, \mathbf{s}, \mathbf{V})$, where $\mathbf{x}$ is the location of a point in the interconnect and $\mathbf{s}$ is the position of any objects responsible for p_k. $\mathbf{V}$ is the vector of all known design parameters (interconnect width, via size, etc.). Then, the location of $\mathcal{B}_j(p_k)$'s boundaries is the locus of all $\mathbf{x}$ that solve

$$\mathcal{P}_n(\mathbf{x}, \mathbf{s_0}, \mathbf{V}) - p_k^{(bound)} = 0\,, \qquad (2)$$

for given object position s_0 and parameter $\mathbf{V}$. As illustration consider the effect of a via structure on the characteristic impedance of a microstrip line. Given the physical dimensions of both objects, a model for the deviation of microstrip impedance $\triangle Z_o$ is derived (Section 2). The resulting space $\mathcal{B}(\triangle Z_o)$ is a two-dimensional sphere centered in s_0 with radius d_0, where d_0 is computed solving Equation (2) for a given constraint $\triangle Z_o^{(bound)}$. Hence any implementations of the microstrip outside this space will satisfy the constraint. Given P_j, the set of all constrained parasitics relevant to net j, $\mathcal{F}_j$ becomes

$$\mathcal{F}_j = \bigcap_{p_k \in P_j} \mathcal{B}_j(p_k)\,.$$

The boundaries of feasibility zone $\mathcal{F}_j$ are often a complex function of relative position and size of the surrounding layout objects and by the constraint imposed on each parasitic p_k as shown in Figure 4 (a) (dotted lines).

If the initial number of bends b exceeds the maximum allocated number the refinement phase terminates. If, on the other hand, $n = N^{(bound)} - b \geq 4$, then the expansion algorithm is applied. Since only Manhattan expansion is allowed, the feasibility zone for each net is horizontally sliced in correspondence of each vertex as shown in Figure 4 (b). Between each pair of horizontal cuts a rectangle is built of width equal to the minimum zone diameter between the cuts. Call R the set of all the rectangles non-adjacent to source and target obtained in this fashion. Since it is preferable to expand interconnect as uniformly as possible in order to keep it at the center of the

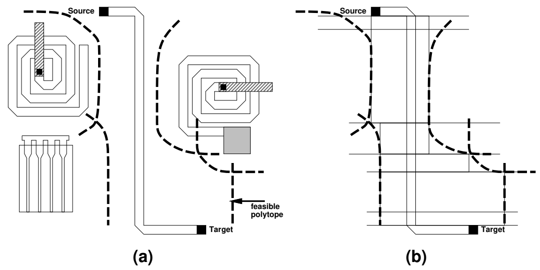


Figure 4: *Distributed parasitics acting on the interconnect determine the feasibility zone.*

zone, the maximum possible number of rectangles r is selected for expansion, where $r = \lfloor \frac{n}{4} \rfloor$. This ensures that the minimum possible horizontal expansion is performed, thus maintaining the distance between interconnect and zone boundary as large as possible. The interconnect can be expanded in two opposite directions in two adjacent rectangles to maximize the length increase $\triangle\ell$, or in two equal direction to minimize the number of bends.

Hence, a large number of combinations for the expansion rectangles exists that obtains the desired expansion. The problem can be formulated as

Find $\overline{R}$, a subset of R, such that the total expansion $\triangle\ell$ is maximized subject to the constraint on number of bends.

This problem can be solved using exhaustive enumeration techniques or linear programming. Due to the low number of vertices per zone, in CORAL the former solution has been adopted.

An expansion step $e = \min_{j \in C} \triangle \ell_j / K$ is selected, where K is a constant proportional to the worst-case number of expansion steps of the algorithm. For each net j the set of all expansion rectangles $\overline{R}_j$ is calculated and each net is expanded by e. The expansion is continued until either a net j reaches its nominal length L_j or a the location of a zone vertex changes. If the first event occurs, net j is dropped from C, e is recomputed and the expansion continues. Otherwise, $\overline{R}_j$ is recomputed for all nets in C and the expansion proceeds until an infeasibility is detected, i.e. interconnect crosses its assigned zone. If the latter case the partially expanded layout is analyzed for performance violations, a new set of weights is generated and routing is repeated. All parasitics responsible for the violation can be easily identified, thus the set of weights associated with these parasitics can be modified so as to insure that a new routing attempt with a modified cost function will reach a satisfactory solution. In our approach, weights are increased by an amount $\triangle w_j^{\cdot}$, inversely proportional to the entity of the violation that the corresponding parasitics induced. m_0 is a normalization factor.

$$\triangle w_j^{\cdot} = \frac{1 - w_j^{\cdot}}{m_0} \sum_{i,f} \left[\frac{S_j^i(f)^-}{\triangle K_i(f)^- - \overline{\triangle K_i(f)^-}} + \frac{S_j^i(f)^+}{\triangle K_i(f)^+ - \overline{\triangle K_i(f)^+}} \right]$$

The sequence of constructive/refinement steps terminates when no more constraint violations are present in the layout or in case the maximum number of iterations is reached.

4 Results

A number of analytical models for MMIC microstrip lines has been computed for the GaAs technology in which the chips were designed. Table 1 shows a

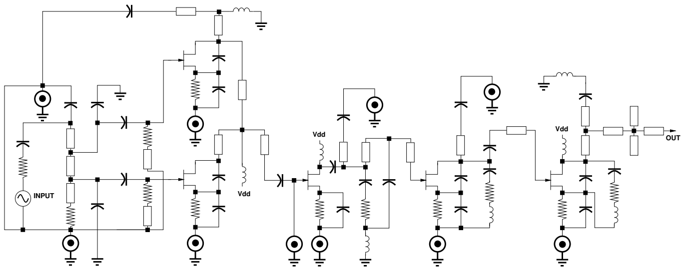


Figure 5: *Schematic of "pcn38".*

Parasitic	parameter	type of model	generation time (sec)
single models			
substrate cap.	C_1	1st ord. polynomial	414.8
cross-over cap.	C_{12}	2nd ord. polynomial	6281.7
parallel line cap.	C_{12}	2nd ord. polynomial	1888.3
char. impedance	Z_w	logarithmic	-
bend	C, L_1, L_2	lumped passive	-
via hole	L_1	1st ord. polynomial	2401.0 (HP9000/750)
correction factors			
adjacent line	$\triangle C_1$	2nd ord. polynomial	3040.9
adjacent pad/spiral	$\triangle Z_w$	2nd ord. polynomial	2543.7
adjacent via	$\triangle Z_w$	2nd ord. polynomial	36 hrs (HP9000/750)

Table 1*: Analytical models used in synthesis for parasitic control.*

Circuit	Frequency range (GHz)	# parasitic constr.	CPU (sec)	specs met
TWA	1-10	39	749	3/3
pcn38	20-40	72	2802	3/3
Wilk	1-20	145	3450	2/2
tq	2-7	131	2991	4/4

Table 2*: Performance of a set of commercial RF benchmarks.*

freq. range (GHz)	25-30	30-35	35-40	40-43
$\lvert S_{11}\rvert$ (dB)	-0.15	-0.03	-0.54	-0.12
$\lvert S_{22}\rvert$ (dB)	+1.22	-1.43	+1.59	+1.24
$\lvert S_{21}\rvert$ (dB)	+0.54	+1.21	+1.57	+0.53

Table 3*: Worst-case performance degradation form nominal of "pcn38".*

summary of the models, along with the CPU time required for their generation on a DECstation 5000/240 (See [9] for a detailed description of the models). The via model required a large CPU time due to the high level of accuracy selected for HFSS in the 3-D field analysis. Notice however that all models have been generated for a given technology, hence no further computational effort is needed for all future designs realized in the same technology.

The routing methodology and the CAD tools described in this paper has been applied to a number of commercial microwave circuits. The circuits were fabricated in HP's GaAs technology and tested. (See Table 2)

The measured performance confirmed the predictions in full with a yield a fraction of a percent lower than that of hand layout. The results of the layout synthesis are shown hereafter in detail for one circuit. The discussion and results of the synthesis of all tested benchmarks can be found in [9].

Consider the three-stage amplifier shown in Figure 5. The specifications are illustrated in Figure 6. All relevant parasitic constraints were generated by PMW in a total CPU time of 2454 sec on a DECstation 5000/240. The

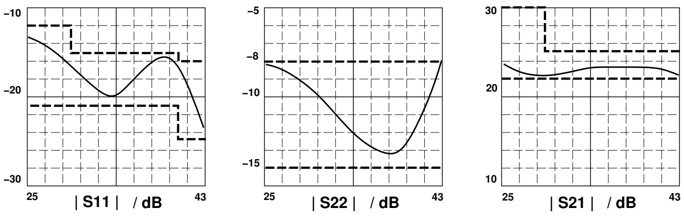


Figure 6*: Performance of "pcn38".*

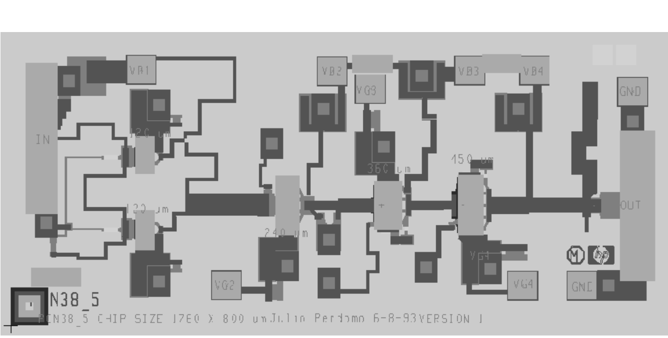


Figure 7*: Final layout of "pcn38".*

computed bounds have then been used by CORAL to route the pre-placed circuit, the resulting layout is shown in Figure 7 and the extracted deviations from nominal performance are listed in Table 3. The CPU time for the routing phase was 348 sec on a DECstation 5000/240. As expected, all performance specifications were met. Figure 6 shows the results of $|S_{11}|$, $|S_{22}|$ and $|S_{21}|$ respectively.

5 Conclusions

A novel technique for the routing of RF and microwave circuits has been proposed. First, sensitivity analysis is performed on the circuit. Using sensitivities and constrained optimization a set of bounds on all critical parasitics in the circuit is generated. These bounds are then directly used by the router, which consists of two phases. During the first phase a sub-set of all constraints is enforced. A cost function drives this routing step where violations to the bounds are weighted differently according to their criticality. During the second phase a refinement is performed on all nets simultaneously so as to enforce all remaining constraints. A final performance verification is performed on the layout. In case one or more violations are detected, the weighting of violations in the cost is modified based on their severity. Routing is iteratively performed until all violations have been eliminated or infeasibility is detected. A number of circuits has been fabricated and successfully tested, thus confirming the suitability of the approach.

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