Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's

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Abstract

This paper presents a new methodology for measuring MOS transistor current mismatch and a new transistor current mismatch model. The new methodology is based on extracting the mismatch information from a fully functional circuit rather than on probing individual devices; this extraction leads to more efficient and more accurate mismatch measurement. The new model characterizes the total mismatch as a sum of two components, one systematic and the other random. For our process, we attribute nearly half of the mismatch to the systematic component, which we model as a linear gradient across the die. Furthermore, we present a new model for the random component of the mismatch which is 60% more accurate, on average, than existing models.

1 Introduction

A good understanding of the matching behavior of components available in a particular integrated circuit technology is critical in designing analog IC's. With the advances in technology leading to smaller feature sizes and more stringent design constraints, device mismatch considerations are becoming increasingly important. An accurate model of transistor mismatch is an integral part of any CAD environment, as it enables the designer to make high-level design trade-offs, such as area of transistor vs. mismatch, or distance between transistors vs. mismatch, at an early stage of the design cycle. It also allows the designer to accurately predict the circuit yield, and possibly to improve that yield through appropriate use of the insight gained from the mismatch models. For example, if we observe that the mismatch has a gradient in a particular direction, then we can place the transistors to be matched perpendicular to that gradient to get better matching. Even though the importance of matching is widely recognized, only a few studies have been conducted to accurately model it.

Mismatch in a certain component can be defined as the variation in the value of identically designed components. Mismatch can be divided into two categories: *random* and *systematic*. Systematic mismatch is that part of the total mismatch where a deterministic trend can be observed in the mismatch values of the various transistors. The remainder of the mismatch, in which no apparent trend is observed, falls under the category of random mismatch.

Some of the causes of transistor current mismatch, as described in [1], are edge effects, implantation and surface state charges, oxide effects and mobility effects. The presence of process gradients causes systematic mismatch in the parameter value of the device. Some of the sources of systematic mismatch, as described in [2], are variations in gate dimensions, gate-oxide thickness gradients, variations in channel doping, and source/drain asymmetry, such as introduced by the tilt angle of ion implants.

Most prior studies have been confined to the modeling of random mismatch. They either ignore the systematic mismatch or model it as an additional normally distributed stochastic process. No attempt has been made in these studies to separate the systematic component from the random component and propose a model for it. We model the systematic component as a $linear$ gradient across the die. The direction of the gradient *is a function of the location of the die on the wafer*. Our study shows that the systematic component accounts for nearly *half* of the total mismatch. We further observe that the direction of the gradient across the die is consistent with a *radial* mismatch pattern across the wafer. With respect to the random component of the mismatch, we propose a model which is *60%* more accurate, on average, than the previous models.

The organization of the paper is as follows. A brief overview of the previous work is found in Section 2. In Section 3 we present our approach of extracting and modeling mismatch, along with the results obtained. Section 4 presents our conclusions.

2 Previous Work

In most of the previous work, either the systematic mismatch is not considered at all [3], [4] or its effect is modeled as a stochastic process with a long correlation distance [1], [5]. In the Fourier domain this effect is modeled as a fixed low frequency contribution with a spatial frequency inversely proportional to the wafer diameter. Normal distribution is considered a reasonable approximation for this [1].

The drain current through a transistor operating in the saturation region is given by

$$I = \frac{K}{2}(V_{GS} - V_T)^2 \tag{1}$$

where I is the drain current, K is the conductance constant, V_T is the threshold voltage, and V_{GS} is the drain-to-source voltage. V_T and K are the statistically significant parameters of this model.

Equation (1) implies that the variance in the drain current is given by

$$\frac{\sigma_I^2}{\bar{I}^2} = \frac{\sigma_K^2}{\bar{K}^2} + 4\frac{\sigma_{V_T}^2}{(V_{GS} - \bar{V}_T)^2} - 4r\frac{\sigma_{V_T}}{(V_{GS} - \bar{V}_T)}\frac{\sigma_K}{\bar{K}} \tag{2}$$

Here, σ_I, σ_{V_T}, and σ_K are the standard deviations of I, V_T and K, respectively. $\bar{I}$, $\bar{K}$, and $\bar{V}_T$ are the expected values of random variables I, K, and V_T, respectively, and r is the coefficient of correlation between V_T and K.

In [4] a model is proposed for σ_K and σ_{V_T} by considering different causes of mismatch. The variance in V_T is modeled by considering the variations in different charge quantities and the gate-oxide capacitance per unit area. Edge effects, variations in channel mobility, and gate-oxide capacitance per unit-area are considered as the causes of mismatch in K. The equations proposed are

$$\frac{\sigma_K^2}{K^2} = k_1(\frac{1}{L^2} + \frac{1}{W^2}) + \frac{k_2}{WL} \tag{3}$$

and

$$\sigma^2_{V_T} = \frac{k_3}{WL}. \quad (4)$$

Here, k_1, k_2, and k_3 are process dependent constants. L and W are the effective lengths and widths of the devices.

For large geometry devices, it is proposed that Equation (3) reduces to

$$\frac{\sigma^2_K}{K^2} = k_1\left(\frac{1}{L^2} + \frac{1}{W^2}\right) \quad (5)$$

It is found that the correlation coefficient, r, is *negligible*.

Pelgrom *et. al.* also propose a similar model by doing analysis in the frequency domain [1]. They show that if the random variations in a parameter, P, are caused by a process which can be modeled as spatial white noise, then the variance of that parameter is inversely proportional to the device area. They then propose that the causes of mismatch in MOS transistor parameters can indeed be modeled as spatial white noise. This leads to a term for mismatch which is inversely proportional to the area of the transistor. Further, they model the systematic mismatch as an additional stochastic process which is normally distributed. This gives rise to a term which depends on the *distance* between two transistors. The final equations for the variance in K and V_T for large geometry devices are

$$\frac{\sigma^2_K}{K^2} = \frac{k_1}{WL} + k_2 D^2 \quad (6)$$

and

$$\sigma^2_{V_T} = \frac{k_3}{WL} + k_4 D^2 \quad (7)$$

Here, k_1, k_2, k_3, and k_4 are process related constants and D is the distance between the pair of rectangular devices to be matched.

Finally, Gregor [2] has reported some work on systematic mismatch, but it is concerned primarily with the causes of mismatch rather than with its modeling.

3 Approach

In this section we first give a description of the mismatch extraction *methodology* used to obtain the mismatch information for this study. We then present the mismatch extraction procedure in Section 3.2. In Section 3.3 we discuss our study of systematic mismatch, followed in Section 3.4 by our model for random mismatch and its comparison with the previous models.

3.1 Extraction Methodology

We propose a new methodology for the measurement of mismatch which is based on the idea that extracting the mismatch information from the observed behavior of a functional circuit is often more efficient and more accurate than individually probing the devices. In this research, for example, transistor mismatch information was extracted from measurements on the D/A converter shown in Figure 1. The converter contains a regular array of transistors, and mismatch between the transistors in this regular array directly manifests itself as integral nonlinearity (INL) errors in the output of the D/A converter. Measurements of these INL errors, therefore, can be used to compute the mismatch of each transistor in the array.

This new methodology is more efficient because no probing of the wafer is required; all measurements can be made by applying various test vectors to the already-packaged chip. Furthermore, the new methodology is more accurate than measuring one device at a time because each component is, in effect, sampled multiple times. In the context of this research, the DAC functions by turning on various combinations of transistors; the output of the DAC for a given input code is the sum of the transistors which are ON for that code. Since each transistor is ON for more than one sample, the current contribution from that transistor is measured multiple times and hence the effective measurement noise is reduced. This effect is similar to measuring a single device multiple times and forming the average of those measurements.

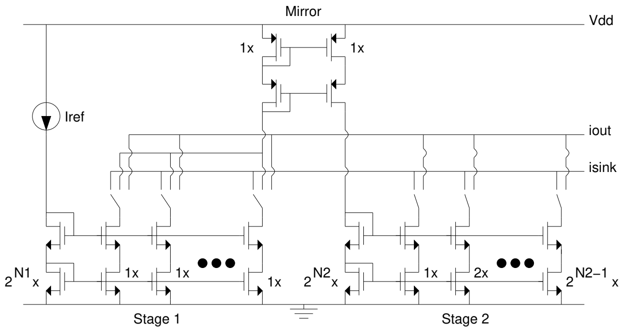


Figure 1: Schematic of D/A converter.

Using this methodology to measure mismatch requires a means for mapping from the observed output of the circuit back to the component mismatches which could have caused that output, since without this mapping it would be impossible to determine the individual component mismatches. This requirement is satisfied by using a behavioral simulator for the system which accurately models mismatch, such as the data converter behavioral model described in [6]. Note that the reverse mapping is particularly straightforward for current-source D/A converters, such as the ones used in this research, as illustrated in Sections 3.2.1 and 3.2.2.

Three different 10-bit DAC architectures were available for this study. All of the architectures are interpolating current-source D/A converters with both unit-weight and binary-weight transistor arrays; the architectures differ in the number of bits in each array. We call the three different architectures DAC46, DAC55, and DAC64. DAC46 has a 4-bit linear array (having 16 transistors) and a 6-bit binary array (having 6 binary-weighted transistors), to give 10 bits. Similarly, DAC55 has 32 transistors in the linear array and 5 binary-weighted transistors in the binary array and DAC64 has 64 transistors in the linear array and 4 binary-weighted transistors in the binary array. All the transistors in the linear array are identical for a given converter. The binary-weighted transistors are implemented by wiring the corresponding number of elemental transistors in parallel. For example, a transistor having a weight of 2X is implemented by switching two identical transistors of weight 1X together, and a transistor of weight 16X is implemented by switching 16 transistors of weight 1X together. The transistors that switch simultaneously in the binary array are arranged in a *common centroid* geometry, so the effect of any linear gradient is canceled and is not reflected in the output. The D/A converters were fabricated through MOSIS on the ORBIT $2.0\mu m$ n-well and p-well processes, as detailed in Table 1. Twelve different chips were available for each of the three DAC architectures. For further details on the design and fabrication of the D/A converters, see [7].

3.2 Extraction of Mismatch Data

The DC transfer curve for each of the D/A converters was exhaustively characterized by attaching the DAC output to a high-gain operational amplifier wired as an I/V converter. All 1024

Chip	Fabrication Process
DAC46	MOSIS 2.0μm, 2 metal, 2 poly, P-WELL (May 93)
DAC55	MOSIS 2.0μm, 2 metal, 2 poly, N-WELL (Feb 93)
DAC64	MOSIS 2.0μm, 2 metal, 2 poly, P-WELL (May 93)

Table 1: Fabrication details for 10 bit D/A converters.

possible inputs were applied to the DAC inputs, and the output corresponding to each input was measured with a high-accuracy voltmeter. Let L represent this transfer curve, where $L[i]$ is the DAC output for input code i. Mismatch values for individual transistors were extracted by using L together with the information about the turn-on sequence of the transistors.

3.2.1 Linear Array

Extraction of the mismatch values for the transistors in the linear array is relatively straightforward. Consider, for example, DAC46. For inputs from $i = 0$ to 63, none of the transistors in the linear array is switched ON, and only the transistors in the binary part are turning ON and OFF (since in DAC46 the six LSB's are implemented in the binary array). Therefore, $L[i]$, for $i = 0$ to 63, reflects the output when none of the transistors in the linear array are turned ON and different transistors in the binary array are switching. For $i = 64$, $L[i]$ represents the output when the first transistor in the linear array is turned ON. Taking the difference $L[64] - L[0]$, we get the contribution of the first transistor to the output. Similarly, $L[128] - L[64]$ represents the current carried by the second transistor that is switched ON in the linear array, and so on. From the DAC schematic and layout we know the turn-on sequence of the transistors, so we can determine the current contributions of the individual transistors in the array. The nominal current for a transistor is taken to be the average current over all the transistors in the linear array. The mismatch is defined as

$$mismatch[i] = actual\_current[i] - nominal\_current \quad (8)$$

Notice that $L[65] - L[1]$, $L[66] - L[2], \ldots, L[127] - L[63]$, all represent the value of current carried by the transistor that switches first in the linear array. By taking the average of all these values, we significantly reduce the noise from our measurements. Since the mismatch is roughly on the same order of magnitude as the measurement noise, this averaging is an important step to improve the accuracy of the measurements.

Exactly the same procedure is applied in case of DAC55 and DAC64 to get the mismatch for the linear array.

3.2.2 Binary Array

Extracting the mismatch information from the binary array is more difficult, since we do not observe the current of any one transistor individually at the output. As an example, consider once again DAC46. $L[1] - L[0]$ represents the value of the current for the the smallest current element. $L[2] - L[0]$ represents the the value when the transistor corresponding to the next significant bit is ON, which actually represents the summed current output of two transistors that are connected in parallel as described in Section 3.1. Similarly, for the next higher bit we observe the sum of four identical transistors placed in parallel. Since the transistors that are used to implement any of the binary-weighted transistors are placed in a common centroid geometry, the effect of any linear gradient is canceled. Therefore only the effect of random mismatch is reflected in the output.

If we assume that each of the unit transistors has a mismatch which is normally distributed with 0 mean and a variance of σ^2, then the sum of the mismatch of two identically designed transistors will be normally distributed with 0 mean and variance of $2\sigma^2$. Similarly, the sum of mismatch of 2^n transistors will be normally distributed with 0 mean and variance of $2^n\sigma^2$. Also, all these distributions are independent, since the transistors being switched ON in each of these cases are different. So, given 12 independent samples (from 12 different dies) from a distribution of $N(0, \sigma^2)$, $N(0, 2\sigma^2)$, $N(0, 4\sigma^2), \ldots$, we wish to estimate the value of σ^2. For this computation, we find the *maximum likelihood estimate* of σ^2 given the values of X_n which are distributed $N(0, 2^{n-1}\sigma^2)$, for $n = 1, 2, \ldots M$. The Joint Probability Distribution function, φ, for these distributions is given by

$$\varphi = \prod_{n=1}^{M} \frac{1}{\sqrt{2^n \pi \sigma^2}} e^{\left(-\frac{X_n^2}{2^n \sigma^2}\right)} \quad (9)$$

Taking the logarithm on both sides and maximizing the $log_e(\varphi)$ w.r.t. σ we get

$$\sigma^2 = \frac{1}{M} \sum_{n=1}^{M} \frac{X_n^2}{2^{n-1}} \quad (10)$$

Using Equation 10 we find the value of σ^2. We obtain a quite accurate estimate of σ^2 because we have a relatively large number of data points: 72 data points (12 dies * 1 value for each of the 6 bits) for DAC46, 60 for DAC55, and 48 for DAC64.

3.3 Study of Systematic Mismatch

3.3.1 Model Used

The systematic component of the mismatch represents that portion of the mismatch which can be precisely predicted, given the process gradients. The random mismatch, on the contrary, represents that portion of the mismatch which is stochastic and hence cannot be predicted. The objective of a mismatch model, therefore, is to maximize the percentage of mismatch which can be systematically predicted and, with regard to the random mismatch, to characterize the σ^2 of the random mismatch as accurately as possible.

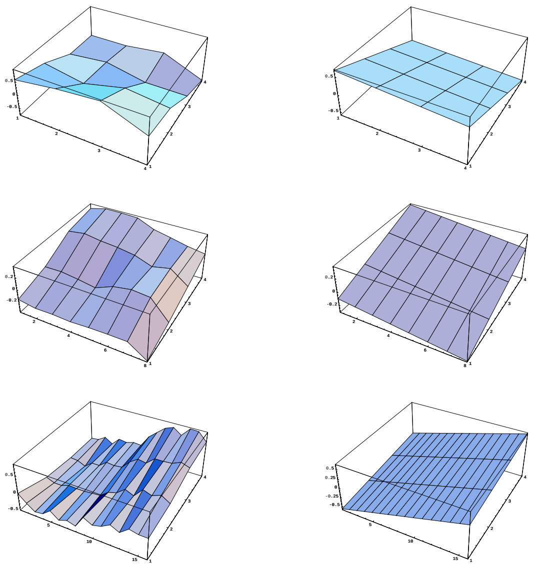
To determine what portion of the mismatch is systematic we generate 3-D plots of the actual mismatch values for the transistor arrays; typical plots are shown in Figure 2. A very strong linear gradient is observed in all the arrays. We model this gradient by a plane which minimizes the mean square error from the actual values. For this we assume that the best fit plane has the form

$$z = lx + my + n \quad (11)$$

The root mean square difference, ε, of the mismatch values from the best fit plane is given by

$$\varepsilon^2 = \frac{1}{N} \sum_{i=1}^{N} (mismatch[i] - lx_i - my_i - n)^2 \quad (12)$$

Here, mismatch[i] is the mismatch value for the i^{th} transistor and N is the total number of transistors in the array.



(a) (b)

Figure 2: (a) 3-D plots of actual intra-die mismatch, for three linear arrays. (b) Systematic mismatch approximated by a linear gradient.

Minimizing Equation 12 w.r.t. l, m, and n, we get

$$-2\sum_{i=1}^{N}(mismatch[i] - lx_i - my_i - n)x_i = 0 \quad (13)$$

$$-2\sum_{i=1}^{N}(mismatch[i] - lx_i - my_i - n)y_i = 0 \quad (14)$$

$$-2\sum_{i=1}^{N}(mismatch[i] - lx_i - my_i - n) = 0 \quad (15)$$

Solving Equations 13, 14 and 15, we get the parameters of the best fit plane.

3.3.2 Results for systematic mismatch

Figure 2(b) shows the plot of the best fit planes corresponding to the plots of actual mismatch in Figure 2(a). We observe that the best fit planes have a large inclination, indicating the importance of the systematic component. Notice that for a completely random mismatch, the best fit plane would be flat. Furthermore, note that these planes are oriented in different directions, so modeling the mismatch as a one-dimensional function of distance would not produce a very accurate model. To make any reasonably accurate predictions about the mismatch we need to know the relative placement of the transistors of interest, the orientation of the best fit plane, and the inclination of the best fit plane.

Upon performing a 2-D FFT analysis on the mismatch matrix, we observe a strong low frequency component. This analysis thus confirms that there is a systematic component of mismatch which varies slowly across the die and can be approximated by a plane.

We calculate the variance of the total mismatch from the best fit plane to get the random mismatch. Table 2 gives the average percentages of mismatch that can be attributed to the systematic and the random parts. We see that roughly 40% of the mismatch, on average, is due to the systematic component.

	avg. % random mismatch	**avg. % systematic mismatch**
DAC46	60.48	39.52
DAC55	50.39	49.61
DAC64	54.16	45.84

Table 2: Systematic vs. Random Mismatch as given by the best fit plane approach.

DAC46	10-bit D/A converter with 16 transistors in the linear array (avg. over 12 dies)
DAC55	10-bit D/A converter with 32 transistors in the linear array (avg. over 12 dies)
DAC64	10-bit D/A converter with 64 transistors in the linear array (avg. over 12 dies)

In Table 3 we present the results of applying the previous model, which treats systematic mismatch as an additional stochastic process (a 1-dimensional function of *distance*), to our data. We see that the contribution of systematic mismatch as indicated by this model is significantly lower than that shown by our approach of modeling it by planes. Thus this model underestimates the true importance of systematic mismatch and falsely classifies it as random mismatch.

	avg. % random mismatch	**avg. % systematic mismatch**
DAC46	66.05	33.95
DAC55	87.39	12.61
DAC64	90.93	9.07

Table 3: Contribution of systematic mismatch by modeling it only as a function of distance.

The next problem in the modeling of systematic mismatch is to find the dependence of systematic mismatch on the position of the die on the wafer, since the direction of the best fit plane is different for different dies. Under the assumption that the origin of systematic mismatch is *deterministic* in nature, it should be possible to predict the direction of the gradient based on the position of the die on the wafer. To model this we would need to know the actual location of each die on the wafer; unfortunately this information is not available for the three D/A converters studied in this paper. The only information that is available is a map of the wafer showing the possible sites for our chips. From this map it is not possible to determine which die belongs to which site on the wafer. Nevertheless, we are able to make a few interesting observations. Figure 3 shows the wafer map from which DAC46 and DAC64 came.

The sites marked 'CA' correspond to our dies. A look at the wafer map shows that all the sites corresponding to our dies lie in the top half of the wafer. Now, a look at the value of the parameters of the best fit planes in Table 4 shows that all the planes for DAC46

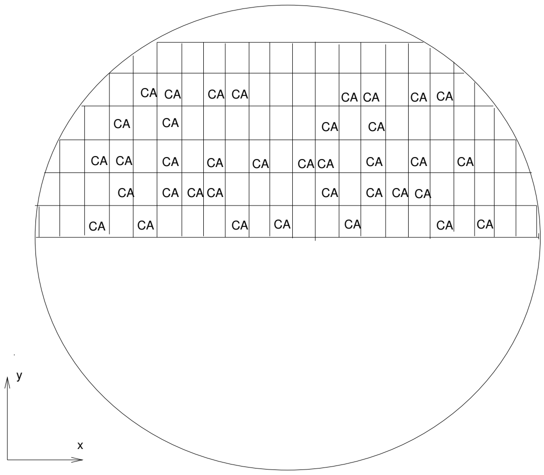


Figure 3: Wafer Map for DAC46 and DAC64.

	DAC46		DAC64	
	x-slope (mm^{-1})	**y-slope** (mm^{-1})	**x-slope** (mm^{-1})	**y-slope** (mm^{-1})
die00	-0.019812	0.001624	-0.002514	0.009489
die01	-0.017729	0.003460	0.003739	0.030543
die02	-0.010549	0.005206	0.001335	0.024435
die03	-0.007312	0.005898	0.001006	0.009303
die04	-0.004454	-0.001771	-0.001075	0.024196
die05	0.030990	0.000009	-0.000658	0.020211
die06	-0.023788	0.005741	-0.001224	0.037188
die07	0.021898	-0.007549	0.001554	0.008030
die08	-0.004108	-0.001221	0.000418	0.012497
die09	0.000764	0.003333	-0.001462	0.009866
die10	0.004325	0.002243	-0.002850	0.011091
die11	-0.010027	0.002527	-0.000118	0.017905

Table 4: Slopes of the best fit planes for DAC46 and DAC64.

and DAC64 have a positive gradient in the y-direction (except for three values in DAC46), while roughly half of the planes have a gradient in the positive x-direction and other half have a gradient in the negative x-direction. If we assume that the dies having opposite x-direction gradients belong to the different sides of the y-axis, then the data is consistent with a radial distribution. For DAC55 the sites were distributed over the entire wafer and no consistent pattern in the directions of the gradients is observed.

3.4 Study of Random Mismatch

Random mismatch is characterized by its variance σ^2, and in this section we propose a model for accurately predicting this variance as a function of $V_{GS}-V_T$ and device area. In Section 3.4.1 we present our model for the random mismatch and in Section 3.4.2 we present the results of using this model and a comparison with the previous models.

Recall that for the binary D/A converters we estimate the variance of random mismatch by using the maximum likelihood estimation criterion. For the linear array we take the difference of the mismatch value from the best fit plane to get the random mismatch. Taking the mean of the square of these values, we obtain the variance of random mismatch. We measured the mismatch values at two different reference currents, 1 mA and 0.6 mA.

3.4.1 Model Used

In this section we propose a modification to the existing models for random mismatch. The drain current in the saturation region is given by

$$I = \frac{K}{2}(V_{GS} - V_T)^2 \tag{16}$$

and the variance in the drain current, ignoring the correlation between V_T and K, can be written as

$$\frac{\sigma_I^2}{\bar{I}^2} = \frac{\sigma_K^2}{\bar{K}^2} + 4\frac{\sigma_{V_T}^2}{(V_{GS} - \bar{V}_T)^2} \tag{17}$$

where σ_K and σ_{V_T} is given by

$$\frac{\sigma_K^2}{K^2} = \frac{k_1}{Area} \tag{18}$$

and

$$\frac{\sigma_{V_T}^2}{(V_{GS} - V_T)^2} = \frac{k_2}{Area(V_{GS} - V_T)^2} + \frac{k_3}{(V_{GS} - V_T)^2} \tag{19}$$

The above model differs from the model proposed in [1] in two ways. First, we do not have any distance-dependent term because we have already accounted for the systematic mismatch. Second, we have added the k_3 term, which does not appear in the Pelgrom model, because in fitting Equation (19) to our data we observed that this k_3 term, which does not contain an area dependence, was much more statistically significant than the corresponding area-dependent term (corresponding to k_2). The addition of this k_3 term leads to an average improvement of nearly 60% as compared to the previous models, as shown in the following section.

3.4.2 Results for Random Mismatch

The values for the various variables in Equations (17), (18), and (19) are shown in Table (5). Equation (16) is used to calculate the nominal value of $V_{GS} - V_T$.

Values of the parameters k_1, k_2, and k_3 were obtained using nonlinear programming. In the nonlinear programming we minimize the square of the difference between the actual and predicted values, subject to the constraint that each of the coefficients must be greater than or equal to 0. The value of k_2 comes out to be zero in our model, validating our claim that the contribution of k_3 is much more significant than the k_2 term.

In Table 5 we present the actual values of σ_I/I vs. the values predicted by our model, along with the percentage errors. The average error from the actual values is approximately 12%. A comparison of our model with that in [1] and [4] is presented in Table 6. In this comparison, only the random part of the total mismatch was used. The mean percentage error is reduced by 60%, from approximately 30% to 12%, by using our model over the previous models.

4 Conclusions

We have proposed both a new method for measuring MOS transistor current mismatch and a new transistor current mismatch model. The conclusions of this study are as follows:

description	# transistors	W (μm)	L (μm)	$area$ (μm^2)	$V_{GS} - V_T$ (V)	measured σ_I/I	predicted σ_I/I	% error
DAC46_lin_1mA	192	121	24	2904	0.679	0.00374	0.00403	+7.75%
DAC46_bin_1mA	768	48	110	5280	0.288	0.01153	0.00922	-20.03%
DAC55_lin_1mA	384	21	24	504	1.163	0.00374	0.00327	-12.56%
DAC55_bin_1mA	384	15	48	720	0.344	0.01005	0.00795	-20.89%
DAC64_lin_1mA	768	28	21	588	0.660	0.00424	0.00457	+7.78%
DAC64_bin_1mA	192	22	47	1034	0.278	0.01029	0.00966	-6.12%
DAC46_lin_0.6mA	192	121	24	2904	0.526	0.00458	0.00514	+12.22%
DAC46_bin_0.6mA	768	48	110	5280	0.223	0.01374	0.01189	-13.46%
DAC64_lin_0.6mA	768	28	21	588	0.511	0.00500	0.00562	+12.4%
DAC64_bin_0.6mA	192	22	47	1034	0.216	0.01300	0.01240	-4.61%

Table 5: Comparison of measured mismatch to predicted mismatch for 10 sets of measurements.

Model Used	Mean percentage error, relative to actual values
Our Model	11.78%
Pelgrom's Model [1]	30.04%
Lakshmikumar's Model [4]	30.44%

Table 6: Comparison of various models for Random Mismatch.

- Transistor current mismatch information can be easily extracted from the regular arrays of transistors in D/A converters.
- Extracting mismatch information from analysis of a functional circuit rather than from individual probing of devices can lead to more efficient and more accurate mismatch measurement.
- The total transistor mismatch should be modeled as the superposition of random mismatch on systematic mismatch.
- The contribution of the systematic component to the total mismatch is as significant as the contribution of the random component. In our circuits the systematic component accounts for approximately 40% of the total mismatch.
- Systematic mismatch can be modeled as a linear gradient across the die, with the direction of the gradient being an important consideration for accurate prediction of mismatch.
- The direction of the gradient depends on the location of the die on the wafer, and our results show that the direction of the gradient is consistent with a radial mismatch pattern.
- Our model for predicting the variance of random mismatch produces approximately 60% more accurate results than the previous models.

5 Future Work

We believe that the methodology we have used to extract transistor mismatch information from D/A converters can be generalized to extracting other parameters of interest from *complex circuits*, as opposed to the common practice of attempting to measure these parameters with special structures and probe pads. Furthermore, we believe that circuits can be specifically optimized to maximize their sensitivity with respect to particular process parameters, and that these specially-optimized circuits would be an efficient and accurate way to measure process parameters.

In addition, we intend to develop a wafer-level model of process gradients. This study of transistor current mismatch has shown that such a model would be very useful in predicting the direction and possibly the incline of the systematic portion of the mismatch.

References

[1] M. J. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching Properties of MOS Transistors", *IEEE J. of Solid-State Circuits*, Vol. 24, No. 5, pp. 1433-1440, Oct. 1989.

[2] R. W. Gregor, "On the Relationship Between Topography and Transistor Matching in an Analog CMOS Technology", *IEEE Transactions on Electron Devices*, Vol. 39, No. 2, pp. 275-282, Feb. 1992.

[3] Jyn-Bang Shyu, G. C. Temes and Francois Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," *IEEE J. of Solid-State Circuits*, Vol. SC-19, No. 6, pp. 948-955, Dec. 1984.

[4] K. R. Lakshmikumar, R. A. Hadaway and M. A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", *IEEE J. of Solid-State Circuits*, Vol. SC-21, No. 6, pp. 1057-1066, Dec. 1986.

[5] Christopher Michael and Mohammed Ismail, "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", *IEEE J. of Solid-State Circuits*, Vol. 27, No. 2, pp. 154-166, Feb. 1992.

[6] E. Liu, A. Sangiovanni-Vincentelli, G. Gielen and P. Gray, "A Behavioral Representation for Nyquist Rate A/D Converters", *Proc. IEEE ICCAD*, pp. 386-389, Nov. 1991.

[7] H. Chang, E. Liu, R. Neff, E. Felt, E. Malavasi, E. Charbon, A. Sangiovanni-Vincentelli and P. R. Gray", "Top-Down, Constraint-Driven Methodology Based Generation of n-bit Interpolative Current Source D/A Converters", *Proc. IEEE CICC*, pp. 369-372, May 1994.

[8] G. Troster and P. Tomaszewski, "Mismatch Simulation for Layout Sensitive Parameters of IC Components and Devices", *IEEE Transactions on Computer-Aided Design*, Vol. 8, No. 2, pp. 101-107, Feb. 1989.