Simultaneous Placement and Module Optimization of Analog ICs

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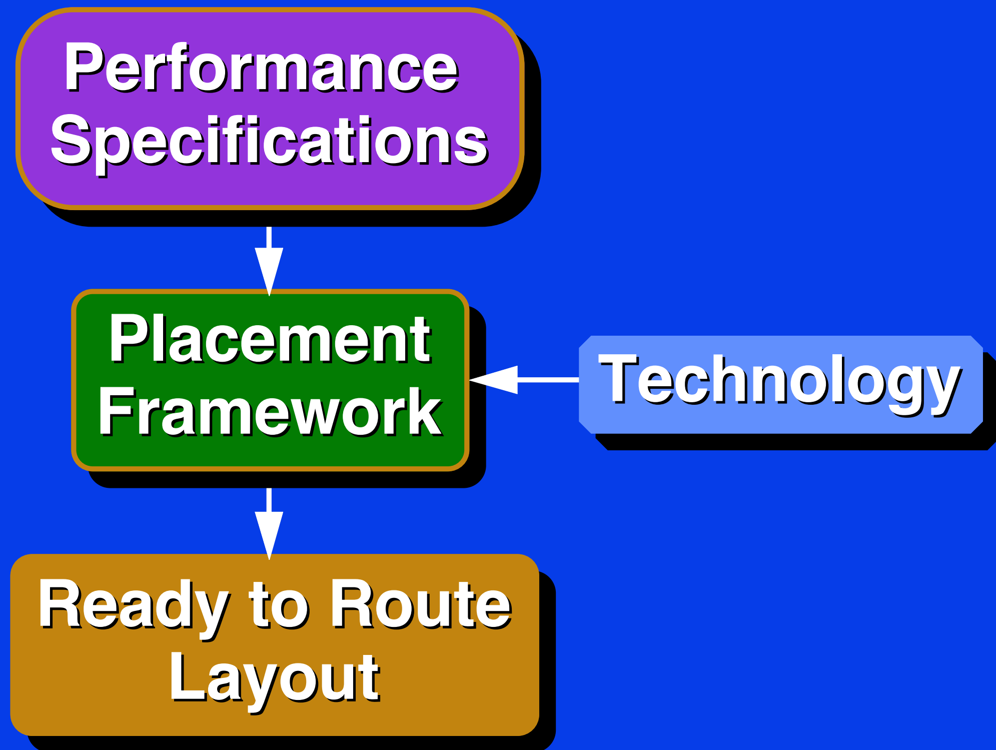
Outline

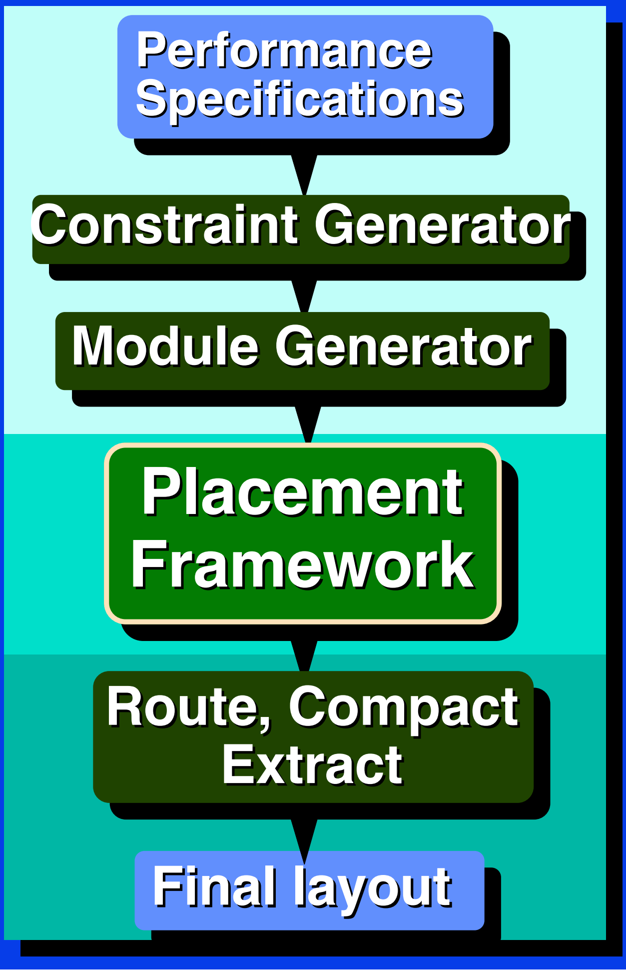
- Objective and background
- Placement framework
- Results
- Conclusions

General Objective



Our Approach: Constraint-Driven Analog Placement

- Part of top-down, constraint-driven methodology [Chang et al. CICC94]
  - → specifications propagated from design level
- Sequential placement, routing, compaction
- Extraction for bottom-up verification

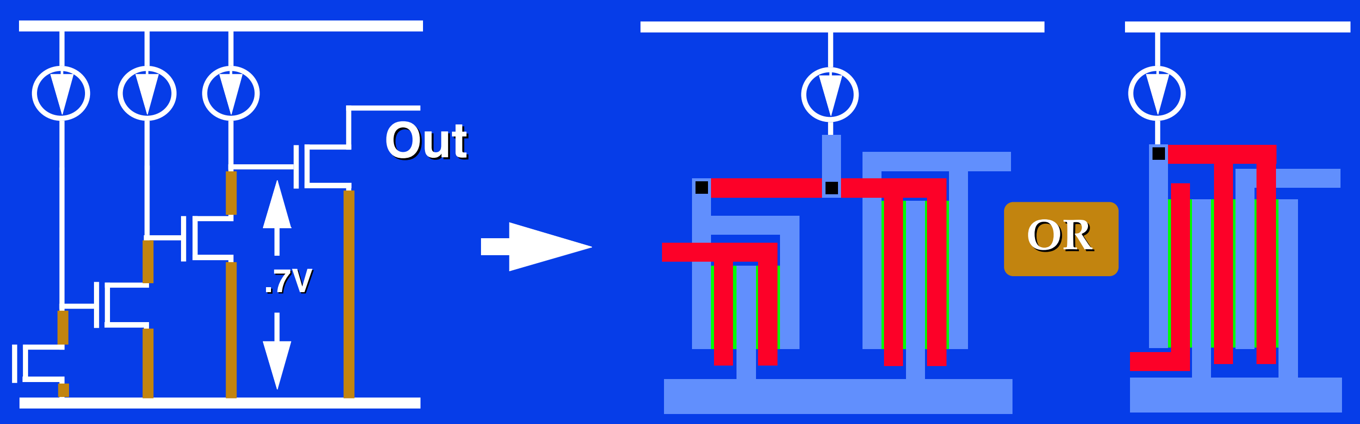


Drawbacks of Sequential Approach

- Independent module generation
  - Module interaction not considered
  - No flexibility in device realization
  - Special configurations (common-centroid, dummy devices, etc.) must be implemented a priori
- Independent routing
  - Need estimations of routing parasitics
  - Relatively low compactness
  - Device mismatch problem

Independent Module Generation

- Parasitic control

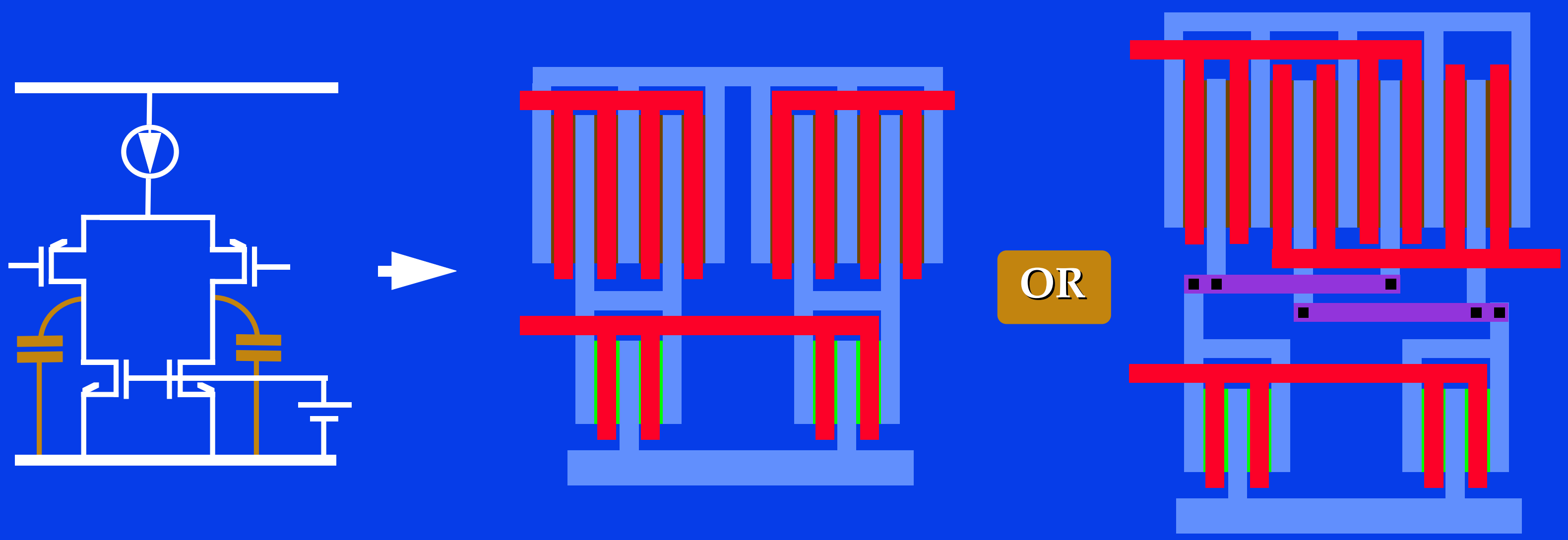


→ Budget parasitics using sensitivities [Choudhury et al. DAC90]

→ Build module(s) according to budgeted parasitics

Independent Module Generation

- Parasitic mismatch control

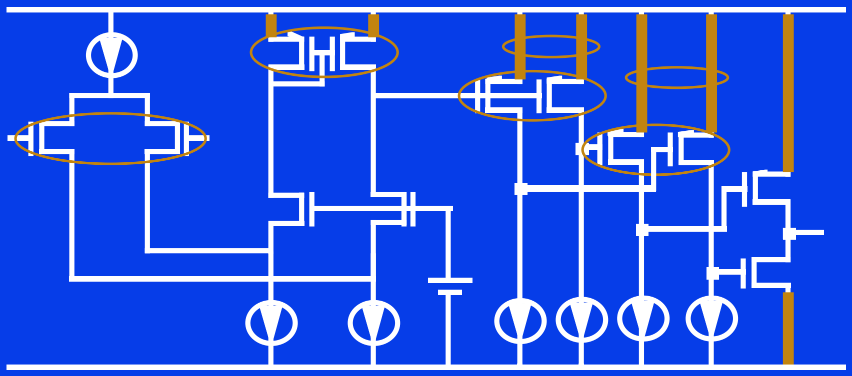


➔ Budget parasitic mismatches [Charbon et al. ICCAD93]

➔ Build modules according to budgeted parasitics

Independent Module Generation

- V_t , R, K' mismatches limit performance
- In extreme cases (low-power design) minimum supply voltage specs might not be met
  - → output range reduction
  - → offset



→ Budget technology mismatches [Charbon et al. ICCAD93]

→ Select special module implementations

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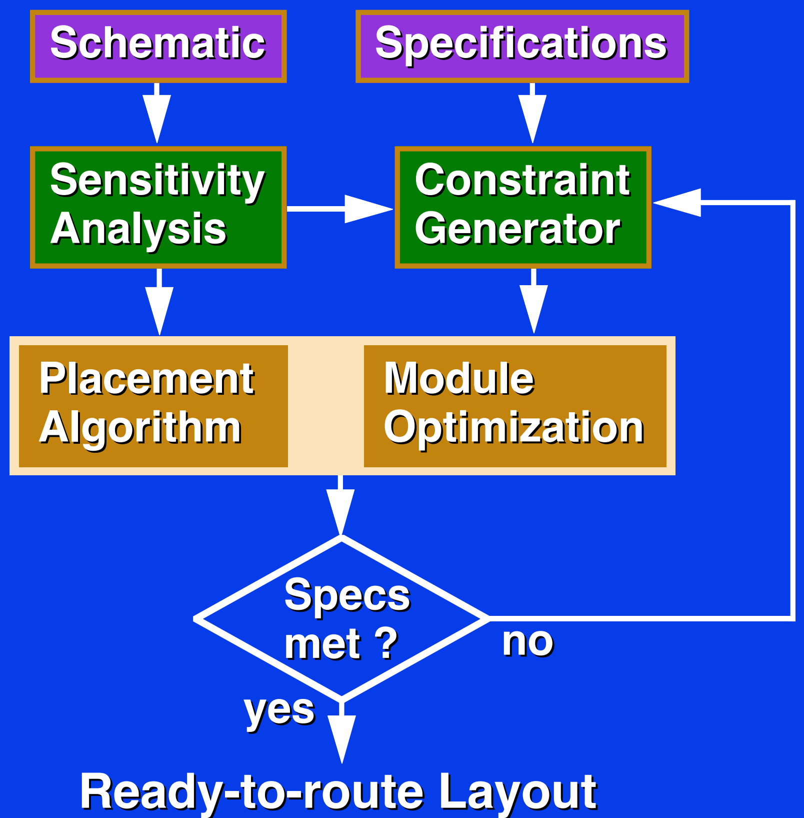
Placement Framework

- Constraint generator produces
  - topological constraints
  - parasitic constraints
- All equivalent solutions generated
- Final selection on modules made during placement
- In case of failure regeneration of constraints or return infeasibility



Module Generation Problem

Goal: find all maximally stacked CMOS module realizations of circuit devices

Subject to:

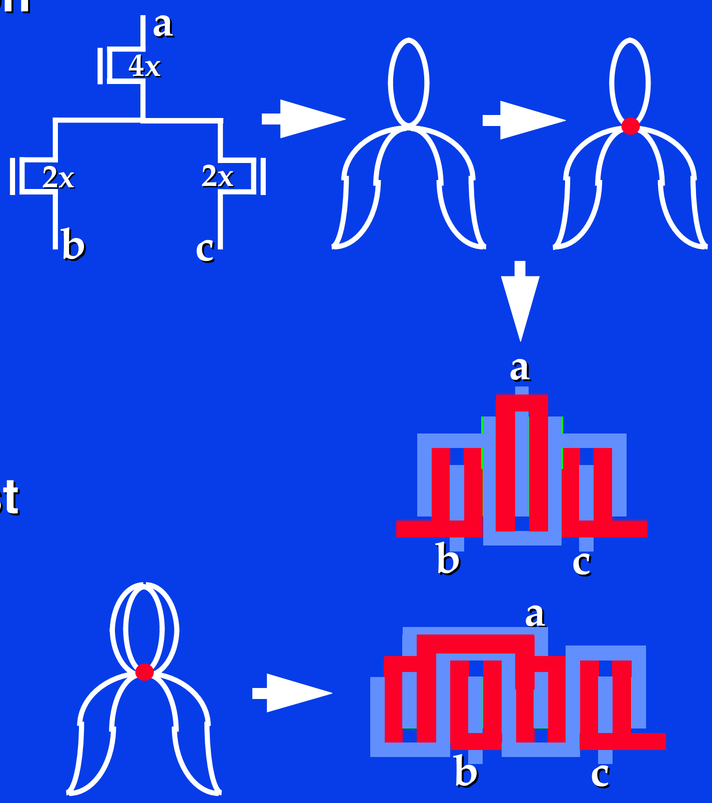
- topological constraints (matching, symmetry)
- parasitic constraints (interconnect)
- parasitic and technology mismatches
- given aspect-ratio range

Proposed heuristics: Chaining Algorithm

→ Problem / Advantage: non-unique solution

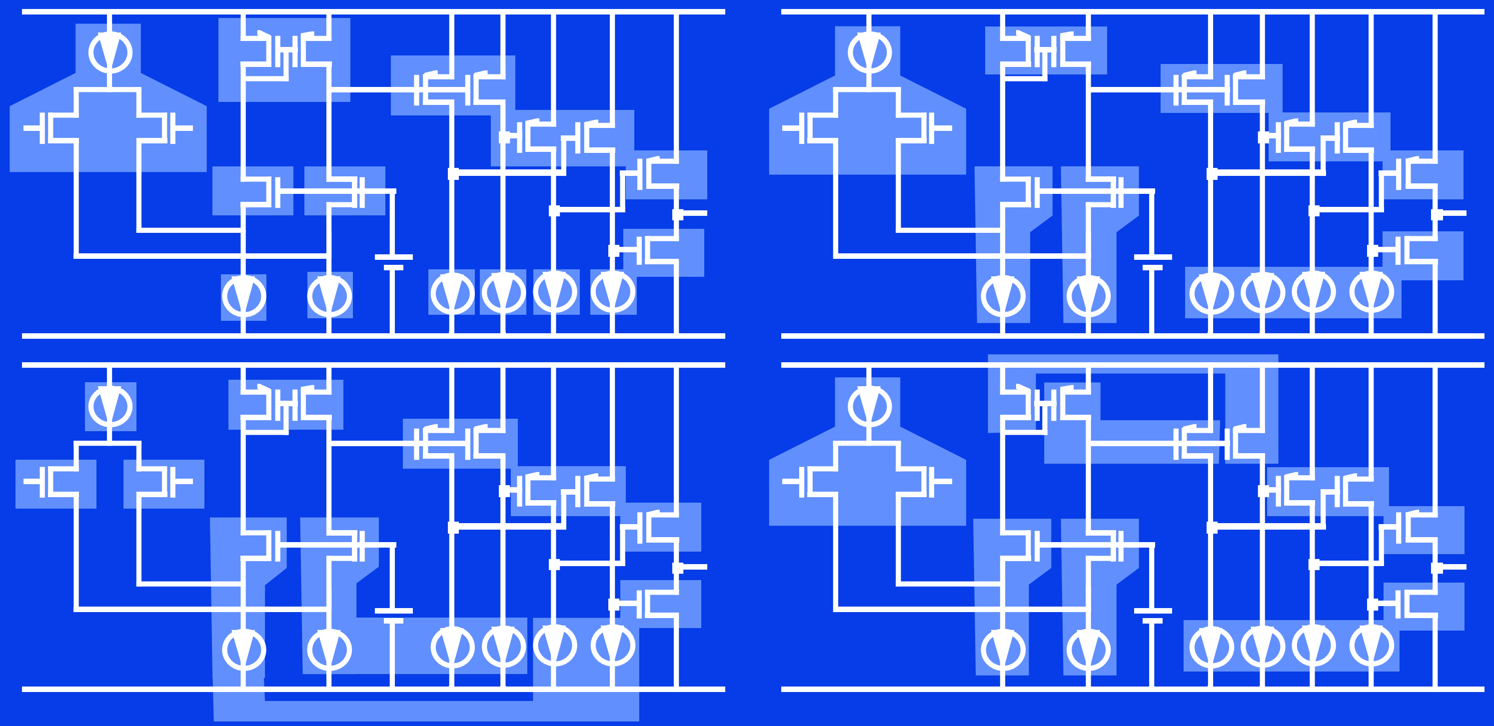
Chaining Algorithm

1. Map devices onto edges of undirected graph
2. Weight nodes based on
   - constraints on parasitic capacitance
   - constraints on stray resistance
3. Enumerate all edge paths (chains) pruning those which violate constraints
4. Evaluate cost (sum of all weights) of each chain and select the one(s) with lowest cost
5. If violations are detected in final chains
   - partition offending modules into smaller edges
   - recursively go to (2)
6. End



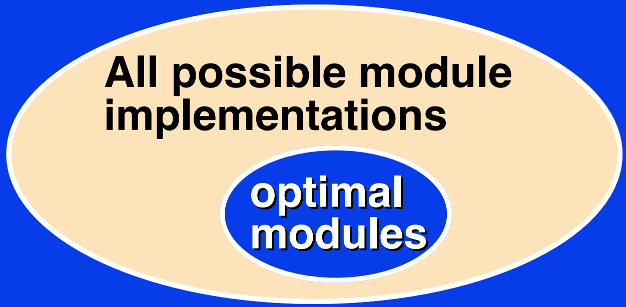
Equivalent Solutions from Module Optimization

- In this example 324 equivalent solutions found
- incomplete information for selection → postpone to placement



Modified Simulated Annealing Placement Algorithm

- Introduce new move (along with tx,rx,xm):
  - swap between equivalent module implementations
- Evaluate impact of implementation on performance
  - estimate all parasitics and mismatches
  - model performance degradation due to parasitics
- Convergence of SA guaranteed [Charbon et al. CICC94]



Evaluation of Alternative Module Implementations

- After each move evaluate violations to specifications
  - → use linear model of performance degradation ΔW based on sensitivities

    $$\Delta W = \sum_i S_i^W \, p_i + \sum_j S_j^W \, \Delta p_j$$

    $S_{i,j}^W$ = sensitivity of W wrt. p_i resp. Δp_j
    p_j = parasitic estimate
    Δp_j = technology / parasitic mismatch

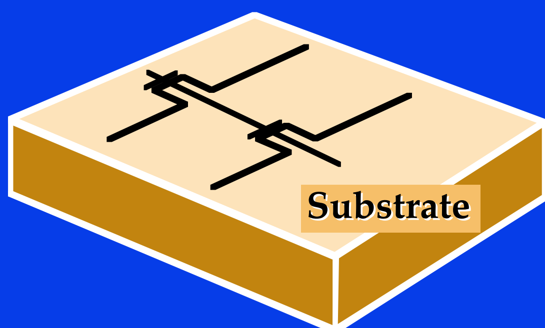
  - → violation to constraint $\Delta W^{(max)}$ (in SA cost function)

    $$F\,(\Delta W^{(max)} - \Delta W)$$

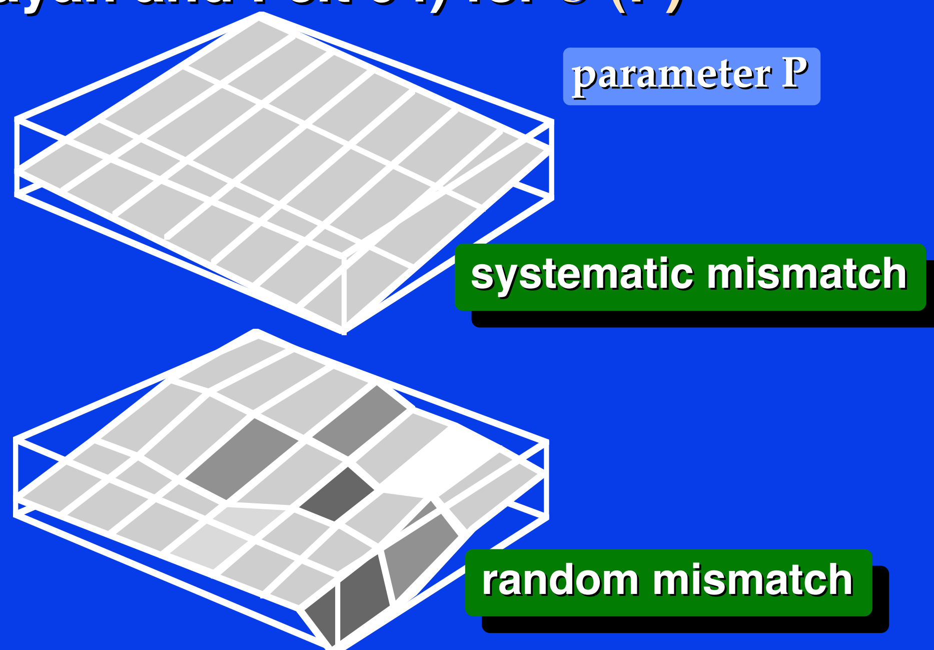
- Need accurate and efficient parasitic estimations

Modeling Parasitics and Technology Mismatch

- Parasitics (R,C,L) estimated through analytical models obtained from detailed field analysis
- Technology mismatch for parameter P (Ex. ΔK, ΔR, ΔV_t, ΔC)
  - → models (Pelgrom 89, Narayan and Felt 94) for $\sigma^2(P)$



$$\sigma^2(P) = \frac{k_1}{Area} + k_2 + \frac{4k_3}{Area(V_{gs}-V_t)^2} + \frac{4k_4}{(V_{gs}-V_t)^2}$$



Advantages of Simultaneous Placement and Module Optimization

- Eliminate one-to-one correspondence device ⇔ module
  → higher implementation flexibility
- Reduce set of realizations for each module
  → decision time during annealing drastically reduced
- Best implementation trade-offs
  → due to better knowledge of layout non-idealities
- Special configurations realized
  → algorithmic generation of interleaved, common-centroid, etc.

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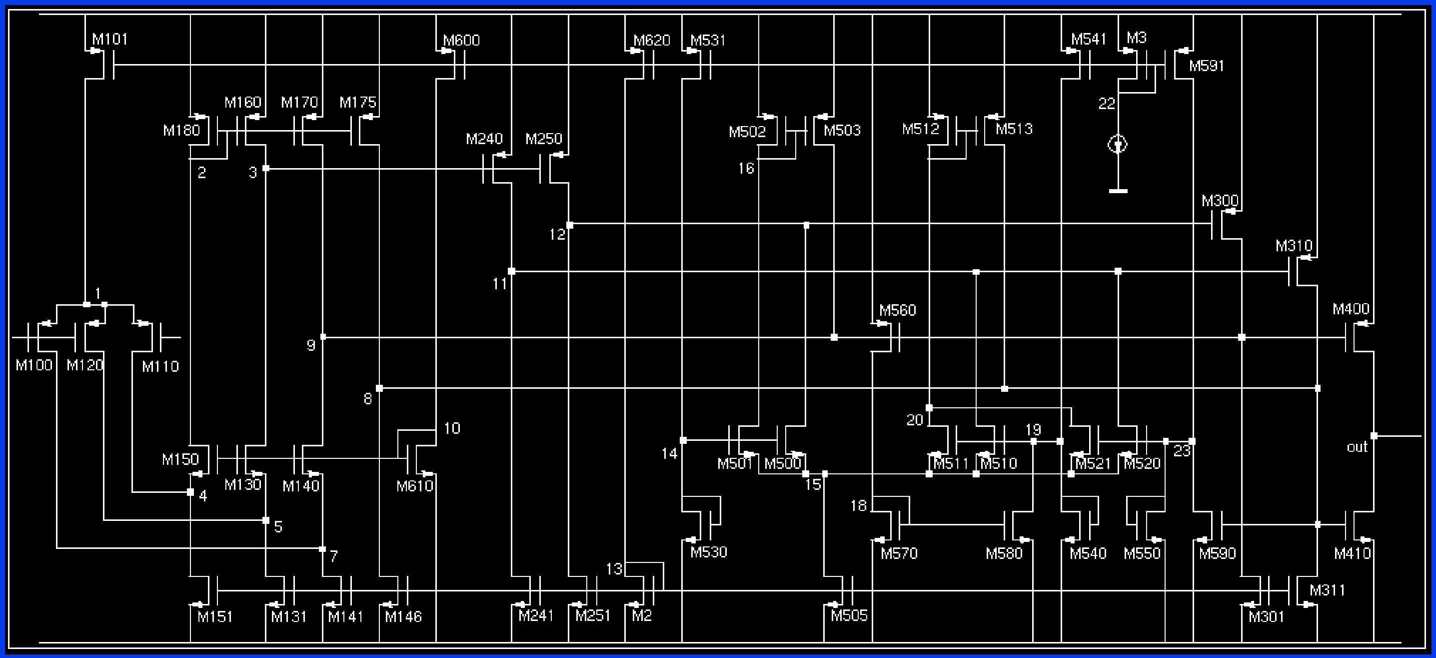
Low-Power Amplifier

Devices

51

Technology

scmos 1μ



R. Eschauzier, R. Hogenvorst and J.H.Huijsing, ISSCC94

Layout

CPU time for constraint-driven layout synthesis

1.75 hrs (placement)
21.0 seconds (mod opt.)
total CPU: 3 hrs

15 days (hand)

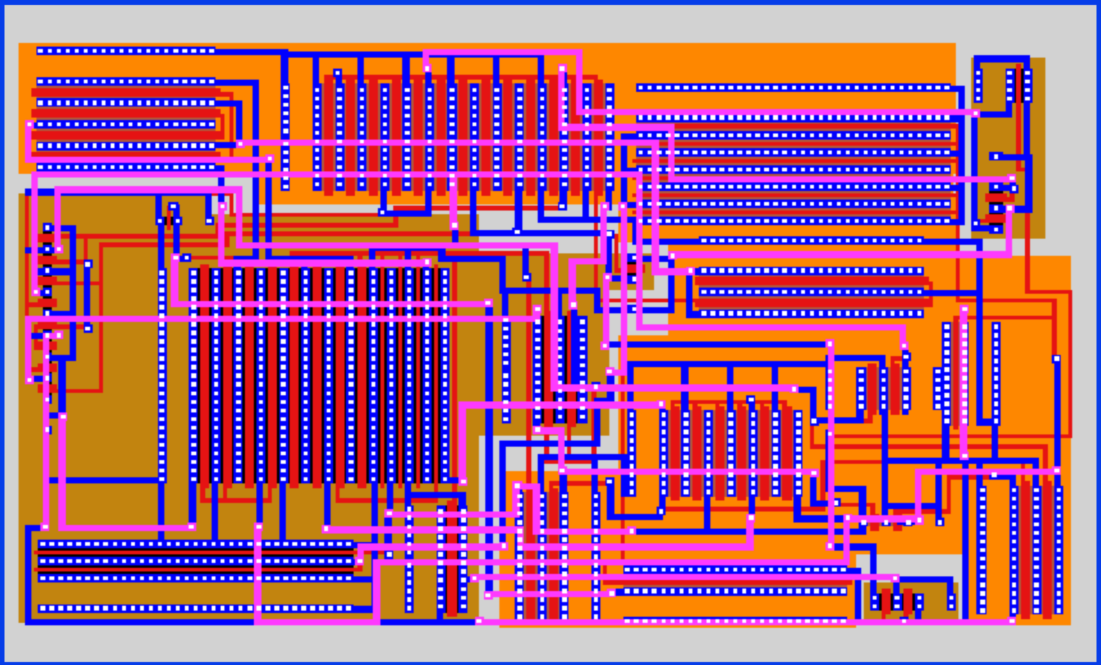
alternative sol.: 324

states visited: 365,565

swaps: 21,494

Acceptance ratio: 0.068

Area: 0.034 mm^2 (auto)
0.028 mm^2 (hand)



Performance

Perform.	Nominal	Specification	Simulated data*
Power	435 μW	+/-130 μW	543 μW
V_{dd}	1.5 V	+/- 0.15 V	full range
LFG	120 dB	- 0.1 dB / +∞	136 dB
UGB	6.0 MHz	- 0.1 MHz /+∞	7.2 MHz
PM	63 °	-/+10 °	56 °

*) Performed with Spice3 (level 3) on fully extracted layout.
Monte Carlo simulation of parasitic mismatches

Analog Benchmarks

Results of performance-driven layout synthesis

Benchmark	# specs	tightness	# sat(P-D)	# sat(no P-D)	CPU (DEC5000125)
fastcomp	3	10%	3	1	442.9
philips	4	1.5%	4	2	1561
ab	4	0.37%	4	3	1552
comp	2	60%	2	1	378
opamp1	4	0.8%	4	2	646
ota731	3	0.16%	2	*	645
mph	5	1%	5	3	6100

Conclusions

- Parasitics and technology mismatches drive module generator
- Equivalent implementations selected during placement based on accurate estimates of layout non-idealities
- Full potential of technology can be used for
  - high-performance, low-power circuits
  - large mixed-signal systems
- Robustness of the approach shown on a large set of industrial circuits