Fall 2001

EE249 Design of Embedded Systems
Homework 1

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Due in class, Oct 2, Tuesday, 10% off for 1 week late

Global hint: make sure you understand the difference between Mealy and Moore FSMs. In particular for Moore FSMs the output relation λ does not depend on the inputs but on the state only (i.e. for a given state the output is fixed independently of the values at the input, so that output and that state are in relation with all possible inputs).

You will need a good amount of time, start soon.

1. **(10 points)** Consider the configuration in Figure 1 showing a Finite State Machine (FSM) M as the composition of two FSMs $M1$ and $M2$. The

Figure 1: Block diagram for Problem 1.

overall specification for M is the following: *"The output y should be 1 if and only if the number of 1's observed in x so far is odd."*. Thus, for input sequence 10011 on x, the sequence of values at y should be 11101. The state transition diagrams of $M1$ and $M2$ are given in Figure 2.

   (a) It is possible to derive a Mealy FSM which replaces $M1$ while having less states?

   (b) If the answer to the previous question is yes, what is the minimum state FSM replacing $M1$?

   (c) Derive a two-state, deterministic Mealy machine that corresponds to the specification for M.

2. **(10 points)** Figure 3 illustrates a sequential logic module M having two inputs x and y and two outputs e and z. The overall specification for M is the following: *e is equal to 1 at clock cycle τ_i if x and y were carrying*

Figure 2: State Transition Diagrams for Problem 1.

the same Boolean value at the previous cycle τ_{i-1}. z *is equal to one at cycle* τ_i *if the output value of* e *at cycle* τ_i *is equal to the output value of* e *at cycle* τ_{i-1}.

Figure 3: Block diagram for Problem 2 - Part 1.

Part 1

(a) Derive the STD of a Mealy Deterministic FSM for M.

(b) Derive the STD of a Moore Deterministic FSM for M.

Figure 4: Block diagram for Problem 2 - Part 2.

Part 2

Consider now the decomposition of module M into modules $M1$ and $M2$ as illustrated in Figure 4. We want to keep the same input/output behavior while designing separately the two modules.

(a) Derive the STDs of two Mealy Deterministic FSMs for $M1$ and $M2$ which together realize the same behavior of M.

(b) Derive the STDs of two Moore Deterministic FSMs for $M1$ and $M2$ which together realize the same behavior of M.

(c) Which conclusions can you derive from this exercise?

3. **(10 points)** Implement and test in Esterel some of the FSMs involved in the exercises above. In particular you should make available (web URL, unix directory in the cad group, e-mail attachment (if anything above fails)) a tar or zip archive containing the tested Esterel source files for

   (a) the communicating $M1$ and $M2$ machines in exercise 1. For $M2$ you should use the STD in Figure 2 and for $M1$ either the machine you derived for part (b) (if such machine exists) or the STD in Figure 2 (if the Mealy machine does not exist).

   (b) the two communicating FSMs, $M1$ and $M2$, in exercise 2, both for the Mealy and the Moore case (sounds like 4 machines). (Hint: playing with Esterel might clarify the differences in the composition of Mealy and Moore machines.)