Welcome to **EE249: Embedded System Design**

*The Real Story*

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*Department of EECS, University of California at Berkeley*
Administration

◆ Office hours: Alberto’s : Tu-Th 12:30pm-2pm or by appointment (2-4882)

◆ Teaching Assistant:

▲ Claudio Pinello, pinello@ic.eecs.berkeley.edu
Grading

◆ Grading will be assigned on:
  ▲ Homeworks (~30%)
  ▲ Project (~50%)
  ▲ Reading assignments (~20%)

◆ There will be approx. 7 homeworks (due 2 weeks after assignment) and 6 reading assignments
Discussion sections

Discussion section:

▲ tool presentation

▲ students’ presentation of selected papers

▼ Each student will have to turn in a one-paragraph report for each paper handed out

▼ Each student (in groups of 2-3 people) will have to make an oral presentation once during the class

Auditors are OK but please register as P-NP

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<th>Discussion Sections</th>
<th>Homeworks</th>
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<td>2</td>
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<td>HW1</td>
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<td>3</td>
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<td>6</td>
<td>Tool presentation</td>
<td>HW3</td>
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Plan

- We are on the edge of a revolution in the way electronics products are designed.
- System design is the key
  - Start with the highest possible level of abstraction (e.g. control algorithms)
  - Establish properties at the right level
  - Use formal models
  - Leverage multiple “scientific” disciplines
- Establish horizontal and vertical “supplier-chain” like partnerships
- Need change in education
Course overview

Managing Complexity

Orthogonalizing concerns

Behavior Vs. Architecture

Computation Vs. Communication
Behavior Vs. Architecture

Models of Computation

Performance models: Emb. SW, comm. and comp. resources

System Behavior

System Architecture

Behavior Simulation

Mapping

Performance Simulation

Communication Refinement

Flow To Implementation

HW/SW partitioning, Scheduling

SW estimation

Synthesis
Behavior Vs. Communication

- Clear separation between functionality and interaction model
- Maximize reuse in different environments, change only interaction model

ETROPOLIS

PIG: Protocol interface generation

PEARLS: Latency insensitive protocols
Outline of the course

- Part 2: Design Methodology
- Part 3: Models of Computation
- Part 4: The Ptolemy, POLIS and VCC Systems
- Part 5: Verification and Synthesis, Hardware and Software
- Part 6: Communication-based Design
Introduction Outline

◆ Scenario and Characteristics of Future Information Technology

◆ Embedded Systems: Automotive, Home Networks, Smart Dusts, Universal Radios

◆ What is Needed at the Infrastructure Level

◆ High-Leverage System Design Paradigms:
  ▲ Communication-based Design
  ▲ Architecture-Function Co-design

◆ Platform-based Design as Implementation Technology
Electronics and the Car

• More than 30% of the cost of a car is now in Electronics
• 90% of all innovations will be based on electronic systems
According to the International Data Corporation

- 96% of all Internet-access devices shipped in the United States in 1997 were PCs.

- By 2002, nearly 50% will not be PCs. Instead, they will be digital set-top boxes, Web-enabled phones, and personal digital assistants, to name just a few.

- By 2004, the unit shipments of such appliances will exceed those of the PC.
Historic Perspective

- Technology discontinuities drive new computing paradigms and applications

- E.g., Xerox Alto
  - 3Ms—1 mips, 1 megapixel, 1 mbps
  - Fourth M: 1 megabyte of memory
  - From time sharing to client-server with display intensive applications

- What will drive the next discontinuity? What are the new metrics of system capability?
What’s Important: Shifts in Technology Metrics

◆ Display (human-computer interface)
  ▲ More ubiquitous I/Os (e.g., MEMS sensors & actuators) and modalities (speech, vision, image)
  ▲ How to Quantify?

◆ Connectivity (computer-computer interface)
  ▲ Not bandwidth but “scaled ubiquity”
  ▲ Million accesses (wired and wireless) per day

◆ Computing (processing capacity)
  ▲ Unbounded capacity & utility functionality (very high mean time to unavailable, gracefully degraded capability acceptable)
What's Important: Shifts in User/Applications Metrics

♦ Cost: Human Effort

▲ Save time
▲ Reduce effort

♦ The Next Power Tools

▲ Leveraging other peoples' effort/expertise

▼ e.g., “What did Dave read about disk prices?”
▼ e.g., “What did people who buy this book also buy?”
Outline

♦ Scenario and Characteristics of Future Information Technology

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  ▲ Architecture-Function Co-design
Chips Everywhere!

Source: Dr. K. Pister, UC Berkeley

Chips that Fly?

SmartPen
## Smart Dust

**Goal:**

- Distributed sensor networks
- Sensor nodes:
  - Autonomous
  - $1\text{mm}^3$

**Challenges:**

- 1 Joule
- 1 kilometer
- 1 piece

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Interface</th>
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<tbody>
<tr>
<td>Power: battery, solar, cap.</td>
<td></td>
</tr>
<tr>
<td>Comm: LOS Optical (CCR, Laser)</td>
<td></td>
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</table>
Smart Dust Components

- Passive CCR comm. MEMS/polysilicon
- Active beam steering laser comm. MEMS/optical quality polysilicon
- Sensor MEMS/bulk, surface, ...

1-2 mm
Airborne Dust

Mapleseed solar cell
MEMS/Hexsil/SOI

Rocket dust
MEMS/Hexsil/SOI

1-5 cm

Controlled auto-rotator
MEMS/Hexsil/SOI
Synthetic Insects
R. Yeh, K. Pister, UCB/BSAC
Computing Revolution: Devices in the eXtreme

Information Appliances: Scaled down desktops, e.g., CarPC, PdaPC, etc.

Evolution

Evolved Desktops

Servers: Scaled-up Desktops,

Revolution

Information Appliances: Many computers per person, MEMs, CCDs, LCDs, connectivity

Servers: Integrated with comms infrastructure; Lots of computing in small footprint

PC Evolution

Display

Mem

µProc

Disk

Display

Mem

µProc

Disk

WAN

Camera

Display

Camera

Display

Info Utility

Computing Revolution
**Modern Vehicles, an Electronic System**

- Electronic Toll Collection
- Collision Avoidance
- Vehicle ID Tracking

**IVHS Infrastructure**
- Cellular Phone
- Navigation
- Info/Comms/AV Bus
- GPS
- Display
- SW Architecture
- Network Design/Analysis

**Multiplexed Systems**
- Body Control
- Suspension
- Vehicle CAN Bus
- ECU
- ABS
- SW Architecture
- Performance Modelling
- Function / Protocol Validation

- Wireless Communications/Data
- Global Positioning
- Electronic Toll Collection
- Collision Avoidance
- Vehicle ID Tracking

- Supplier Chain Integration
**Challenges**

- Minimum Technology to Satisfy User Requirement
- Usability
- Integrate with Other Vehicle Systems
- Add the Function Without Adding the Cost
When Will Dick Tracy’s Watch Be Available?

Ultimate Nomadic Tool in Broadband Age

- Two-way Communication
- Language Translation & Interpretation
- e-Secretary
- Camera
- Music
- Electronic Money
Smart Buildings

- Disaster mitigation, traffic management and control
- Integrated patient monitoring, diagnostics, and drug administration
- Automated manufacturing and intelligent assembly
- Toys, Interactive Musea

Dense wireless network of sensor, monitor, and actuator nodes

-Localized zones, to be individually controlled by building occupants, creating "micro-climates within a building"

- Other functions: security, identification and personalization, object tagging, seismic monitoring
Home Networking: Application (Subnet) Clusters

PC/Data Based
- PC-1
- PC-2
- Printer
- Internet Access

Entertainment Based
- TV
- Stereo
- Cam Corder
- DVD Player
- VCR
- Video Game

Appliance Based
- Sprinklers
- Toasters
- Ovens
- Clocks
- Utility Customization
- Climate Control

Security Based
- Door Sensors
- Motion Detectors
- Window Sensors
- Video surveillance
- Smoke Detectors
- Audio Alarms
- Light Control

Telecom Based
- Voice Phone
- Video Phone
- PDA
- Intercom

Entertainment Based
- Still Camera
- Web-TV STB
Silicon-Processed Micro-needles

- Neural probe with fluid channel for bio-medical appl.
- Two micro-needles penetrating porterhouse (New-York) steak

**Industrial Structure Shift**

- **Market Structure Shift**
  - Personal/Internet/Terminal
  - Cellular
  - Game Machine

- **LSI Market Size**
  - (B$)
  - World Wide Semiconductor Market Size
  - SoC Market Size

- **SOC Era has come.**

- **Current Percentage of SoC Ratio is under 10%.**
  → 40% in 2005, 70~80% in 2010

- **SoC is “single-seat constituency”, “take or not”.**

- **Key Factor is the Synergy between Semiconductor & Set Divisions.**

- **Shift of Technology Driver**
  - PC → DC
  - Wintel → Non-Wintel

- **90’s**
  - PC → High Performance ~ Game Machine
  - Low Power ~ Cellular

- **00’s**
  - PC → Low Power ~ Cellular
  - Game Machine ~ Internet/Terminal

- **Key Factor:** The Synergy between Semiconductor & Set Divisions.
Productivity Gap

Potential Design Complexity and Designer Productivity

- Logic Tr./Chip
- Tr./S. M.

58%/Yr. compounded Complexity growth rate
21%/Yr. compounded Productivity growth rate

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology</th>
<th>Chip Complexity</th>
<th>Frequency</th>
<th>3 Yr. Design Staff</th>
<th>Staff Cost*</th>
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<tr>
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<td>400</td>
<td>210</td>
<td>90 M</td>
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<td>1998</td>
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<td>270</td>
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<td>1999</td>
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<td>32 M Tr.</td>
<td>600</td>
<td>360</td>
<td>160 M</td>
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<td>2002</td>
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<td>130 M Tr.</td>
<td>800</td>
<td>800</td>
<td>360 M</td>
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* @ $150K / StaffYr. (In 1997 Dollars)
The Berkeley Wireless Research Center (BWRC)

♦ Brodersen, Rabaey, Gray, Meyer, Katz, ASV, Tse and students

♦ Cadence, Ericsson, HP, Intel, Lucent, ST, TI, Qualcomm

♦ Next Generation Wireless systems:
  ▲ Circuits
  ▲ Architectures
  ▲ Protocols
  ▲ Design Methodologies
The “Universal” Radio

Fourth-generation radio providing following features

- Focus on the wireless services with minimal constraints on how the link is provided
- Allows for uncoordinated co-existence of service providers (assuming they provide compatible services)
- Provides evolving functionality
  ▲ Adapts to provide requested service given type of service, location, and dynamic variations in environment (i.e. number of users)
  ▲ Allows for to continuously upgrade to support new services as well as advances in communication engineering and implementation technologies

Presents an architectural vision to the multi-user, multi-service problem!

- This is in contrast with current approach where standards are the input and architecture the result - leading to spectral wasteland
Ultra Low-Power PicoRadio

- Dedicated radio’s for ubiquitous wireless data acquisition and display.
  Energy dissipation and footprint are of uttermost importance
- Goal: P < 1 mW enabling energy scavenging and self-powering
- Challenges:
  ▲ System architecture: self-configuring and fool-proof
  ▲ Ultra-low-power design
  ▲ Automated generation of application-specific radio modules making extensive use of parameterizable module generators and reusable components
Integrate within the same chip very diverse system functions like: wireless channel control, signal processing, codec algorithms, radio modems, RF transceivers… and implement them using a heterogeneous architecture.
Communication versus Computation

- Computation cost (2004): 60 pJ/operation (assuming continued scaling)

- Communication cost (minimum):
  - 100 m distance: 20 nJ/bit @ 1.5 GHz
  - 10 m distance: 2 pJ/bit @ 1.5 GHz

- Computation versus Communications
  - 100 m distance: 300 operations = 1 bit
  - 10 m distance: 0.03 operation = 1 bit

Computation/Communication requirements vary with distance, data type, and environment
“Software-defined Radio”
Outline

- Scenario and Characteristics of Future Information Technology
- Embedded Systems: Automotive, Home Networks, Smart Dusts, Universal Radios
- What is Needed at the Infrastructure Level
- High-Leverage System Design Paradigms:
  - Communication-based Design
  - Architecture-Function Co-design
- Platform-based Design as Implementation Technology
What is Needed?
(Endeavor Expedition, Berkeley Oxygen, MIT)

◆ Automatic Self-Configuration
  ▲ Personalization on a Vast Scale
  ▲ Plug-and-Play

◆ The OS of the Planet
  ▲ New management concerns: protection, information utility, not scheduling the processor
  ▲ What is the OS of the Internet? TCP plus queue scheduling in routers

◆ Adapts to You
  ▲ Protection, Organization, Preferences by Example
Technology Changes & Architectural Implications

- Zillions of Tiny Devices
  - Proliferation of information appliances, MEMS, etc.
- “Of course it’s connected!”
  - Cheap, ample bandwidth
  - “Always on” networking
- Vast (Technical) Capacity
  - Scalable computing in the infrastructure
  - Rapid decline in processing, memory, & storage cost

- Adaptive Self-Configuration
- Loosely Organized
- “Good Enough” Reliability and Availability
- Any-to-Any Transducers (dealing with heterogeneity, over time–legacy–and space)
- Communities (sharing)
Adaptive Self-Configuration

♦ Plug-and-Play Networking
  ▲ No single protocol/API: standardization processes too slow and stifle innovation
  ▲ Devices probe local environment and configure to inter-operate in that environment
  ▲ “Computer” not defined by the physical box: portals and ensembles

♦ Local Storage is a Cache
  ▲ Invoke software and apps migrate to local disk

♦ System Learns Preferences by Observation
  ▲ E.g., “Privacy by Example:” owner intervention on first access, observe and learn classification, reduce explicit intervention over time
Loose Organization

- **Loosely Structured Information**
  - Large volume, easily shared: supports communities

- **Self-Organized**
  - Too time consuming to do yourself: Organize by example
  - Individualized & context-dependent filtering

- **Incremental Access, Eventually exact**
  - Query by concept: “What did Dave read about storage prices?”
    - “A close answer quickly is better than a precise answer in the far future”;
    - Probabilistic access is often “good enough”
Any-to-Any Transducers

- No need for agreed upon/standardized APIs (though standard data types are useful)
  - If applications cannot adapt, then generate transducers in the infrastructure automatically
  - Exploits compiler technology
  - Enhance plug-and-play to the application level

- Legacy Support
  - Old file types and applications retained in the infrastructure
Advances in hardware and networking will enable an entirely new kind of operating system, which will raise the level of abstraction significantly for users and developers.

Such systems will enforce extreme location transparency:
- Any code fragment runs anywhere
- Any data object might live anywhere
- System manages locality, replication, and migration of computation and data

Self-configuring, self-monitoring, self-tuning, scaleable and secure

Adapted from Microsoft “Millenium” White Paper
http://www.research.microsoft.com
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**Issues Limiting SOC Ramp**

- Economics
- Productivity
- Process
- IP Delivery & Reuse
- Tools & Methodology
- Manufacturing

**How do we move SoC Design from the pilot line to production?**

Source: M. Pinto, CTO, Lucent MT
SoC Landscape 2000+

- Total Cost Ownership
  - Average cost of a high end ASSP >$5M
  - Cost of fabrication and mask making has increased significantly ($500k+ for masks alone)
  - SoC/ASIC companies look for a 5-10x return on development costs (~$10M revenue)
  - Shorter and more uncertain product life cycles

- Compounding Complexities limiting Time-to-Market
  - Chip design complexity
  - Silicon process complexity
  - Context complexity
  - End-to-end verification

- New “System to Silicon” methodologies are required that recognized 80% of the system development is software

Source: M. Pinto, CTO, Lucent MT
Will the design team deliver on time and within budget?

Source: M. Pinto, CTO, Lucent MT
**Process Challenge**

Can you integrate what you need?

**Lucent Modular Process Strategy**

- Communications focus
- IP re-use across businesses
- Flexible system partitioning
- Only pay for what you need
- Leverage high volume platform
- Manufacture at fabs worldwide

Source: M. Pinto, CTO, Lucent MT
Manufacturing Paradigm Challenge

Interconnection Dominates Fabrication Throughput

% of Fab of Interconnection vs. % of Fab Up-to-Contact

- Drives the need for new rapid prototype and production techniques
- Impacts industry spare gate methodology for quick fixes
- All metal programmable option lose their time to market advantage

Source: M. Pinto, CTO, Lucent MT
Deep Submicron Paradigm Shift

- 2M Transistors
- 100M Metal
- 100 MHz
- Wire RC 1 ns/cm

- 40M Transistors
- 2,000M Metal
- 600 MHz
- Wire RC 6 ns/cm

Cell Based Design
- Minimize Area
- Maximize Performance
- Optimize Gate Level

Virtual Component Based Design
- Minimize Design Time
- Maximize IP Reuse
- Optimize System Level
Deep Sub-Micron: Impact on Semicon Industry

- Today, several IC companies have a chance of selling their devices on a board.
- With the possibility of integrating an entire system on a single chip, there will be room only for one manufacturer!!!
- However, nobody can possibly know all these areas in depth.
Virtual Components and System Design

- Select the best components from several different internal and external vendors
- Integrate the system using standard interfaces
- Validate the design functionality, performance and reliability.
Industry Structure: Tomorrow

System

Product Definition Marketing

Implementation, IP Selection and Certification

Chip, Substrate, Board Assembly

Architectural Design and Assembly

Manufacturing

IP Providers
SoC Economic Challenge “2000+”

Platform Technology lowers the cost of entry and accelerates time-to-market

Source: M. Pinto, CTO, Lucent MT
Implementation Design Trends

- **Platform Based**
  - Consumer
  - Wireless
  - Automotive

- **Hierarchical**
  - Microprocessors
  - High end servers
  & W/S

- **Flat Layout**
  - Net & Compute
  - Servers
  - Base stations

- **EDA**
- **Flat ASIC**
- **MicroP**
- **Flat ASIC+**
ASIC in Computers & Servers, still flat today

♦ ASIC in 1999: 3.7 Million Gates high end, some mid range
  ▲ “Most of Sun’s ASIC have outgrown the capabilities of flat timing free layout design methodologies”

ASIC in 2000: 5 M gates + 1.5-2M Memory, 300-500 MHz
  • “hierarchy the norm and not the exception”
  • “trial layout giving way to iterative physical chip integration”

Source: Sun Microsystems-DS99
Digital Wireless Platform

Source: Berkeley Wireless Research Center
Will the system solution match the original system spec?

Concept

- Limited synergies between HW & SW teams
- Long complex flows in which teams do not reconcile efforts until the end
- High degree of risk that devices will be fully functional

- Development
- Verification
- System Test

IP Selection
- Design
- Verification

Software

Hardware

Limited synergies between HW & SW teams
Long complex flows in which teams do not reconcile efforts until the end
High degree of risk that devices will be fully functional
**EDA Challenge to Close the Gap (SIA MARCO GSRC Project, Berkeley Center)**

- Industry averaging 2-3 iterations SoC design
- Need to identify design issues earlier
- Gap between concept and logical / Physical implementation

![Diagram](image)

- **Level of Abstraction**
  - Behavior
  - SW/HW
  - RTL
  - Silicon

- **Impact of Design Change**
  - (Effort/Cost)

- **Concept to Reality Gap**
- **Design Entry Level**
- **Historical EDA Focus**

Source: GSRC
What is a *System* Anyway?
System (for us)

- Environment to environment

- Sensors + Information Processing + Actuators
  - Computer is a system
  - Micro-processor is not


Embedded Systems

◆ Non User-Programmable

◆ Based on programmable components (e.g. Microcontrollers, DSPs...)

◆ Reactive Real-Time Systems:
  ▲ “React” to external environment
  ▲ Maintain permanent interaction
  ▲ Ideally never terminate
  ▲ Are subject to external timing constraints (real-time)
The New IC Micro-system

- Assembly of “prefabricated component” often purchased from external vendors (“IP”)
  - “black box” hierarchy
- Design & Verification at the System level
  - rather than the logic level
  - Interface and communication
- Great Importance of Software
**Design Methodology Progression**

- **Technology Independent**
  - HDLs
  - Micro-architecture
  - Development tools (SmartLibs, MPEG)
  - System on a Chip
- **Technology Dependent**
  - Schematics
  - Integration
  - Design tools (MPEG, Block-based design)

This diagram illustrates the progression from technology-independent to technology-dependent methodologies in design.
Block Based Design
Types of Virtual Components

**Firm VC**
- Gate level or Synthesizable RT level data
- Some Technology and/or Physical constraints
- Some flexibility on Form and Function
- Predictable size and speed

**Hard VC**
- Polygon level data
- Technology Specific
- Fixed Form & Function
- Well characterized

**Soft VC**
- RT Level or above
- Technology Portable
- Flexible Form & Function
- Estimated size and speed
Alliance Vision... Intra- and Inter-Company World Wide IP Networks

System House Corporate Headquarters

Rapid IP Identification, Business Transaction, & Design-in

Overseas Affiliate with Proprietary IP

Semiconductor & IP Provider

Independent IP Provider