Noise Considerations in Circuit Optimization

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Abstract

Noise can cause digital circuits to switch incorrectly and thus produce spurious results. Noise can also have adverse power, timing and reliability effects. Dynamic logic is particularly susceptible to charge-sharing and coupling noise. Thus the design and optimization of a circuit should take noise considerations into account. Such considerations are typically stated as semi-infinite constraints. In addition, the number of signals to be checked and the number of sub-intervals of time during which the checking must be performed can potentially be very large. Thus, the practical incorporation of noise constraints during circuit optimization is a hitherto unsolved problem.

This paper describes a novel method for incorporating noise considerations during automatic circuit optimization. Semi-infinite constraints representing noise considerations are first converted to ordinary equality constraints involving time integrals, which are readily computed in the context of circuit optimization based on time-domain simulation. Next, the gradients of these integrals are computed by the adjoint method. By using an augmented Lagrangian optimization merit function, the adjoint method is applied to compute all the necessary gradients required for optimization in a single adjoint analysis, no matter how many noise measurements are considered and irrespective of the dimensionality of the problem. Numerical results are presented.

1 Introduction

In the context of digital circuits, noise is defined as any deviation of a signal from its stable value in those subintervals of time when it should otherwise be stable [1]. Noise in digital circuits can be attributed to several sources such as leakage noise, charge-sharing noise, crosstalk noise, power supply noise, shot noise, thermal noise and flicker noise. Rigorous noise analysis and noise considerations during design are becoming increasingly important. The following trends in modern digital integrated circuit design accentuate the need for careful and detailed consideration of noise during circuit design and optimization.

- Supply voltages are being lowered, leading to smaller margins for noise.
- Transistor threshold voltages are being lowered, leading to higher levels of leakage noise.
- Circuits are being packed closer together, leading to increased coupling and cross-talk noise.
- Signals have faster rise and fall times, leading to more power supply noise.
- The increased use of dynamic circuitry for performance reasons worsens the susceptibility to noise problems. Charge-sharing noise problems are often avoided by appropriate sizing of transistors.

When a circuit is optimized, noise should be considered in addition to such criteria as delay, power and area. The mathematical expression of noise considerations in circuit optimization is in the form of a nonlinear semi-infinite problem [2, 3]. In addition, the number of signals that must be checked for noise violations and the number of sub-intervals of time during which these checks must be performed are potentially very large. Hence the incorporation of noise considerations during circuit optimization is an arduous task and no practical solution exists in the literature.

This paper presents a method for efficiently incorporating noise considerations during circuit optimization based on time-domain simulation. The semi-infinite noise considerations are first mapped into equality constraints involving time integrals. The time integrals are computed during the simulation in the inner loop of the optimizer. The time integral form of the resulting equality constraint lends itself well to gradient computation by the adjoint method [4]. By exploiting the fact that the optimizer builds a scalar merit function, all the gradients of the merit function

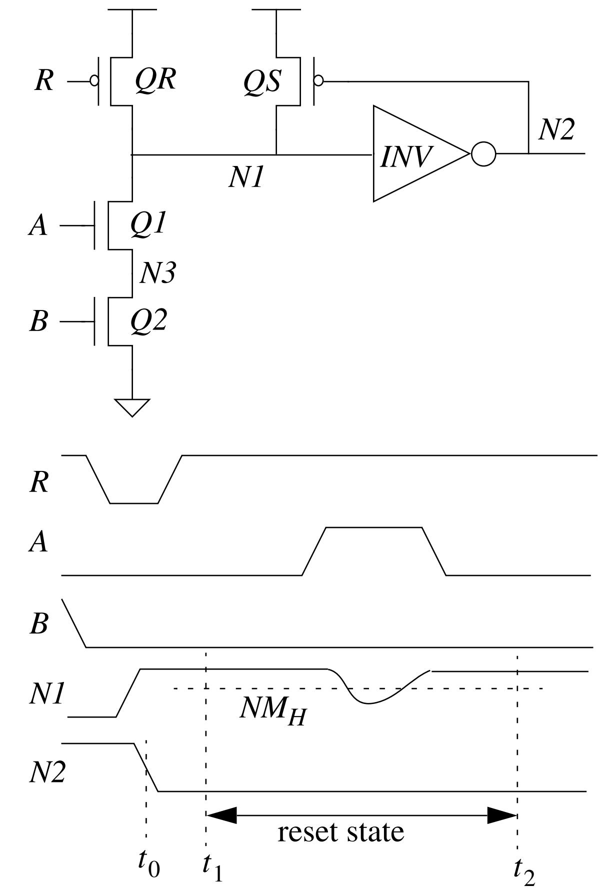

Figure 1: Dynamic circuit susceptible to charge-sharing noise and associated waveforms.

are computed in a single adjoint analysis [5, 6], thus rendering the procedure tractable. Prototype software to tune transistor and wire sizes while taking into account noise, delay, slew, power and area considerations has been developed.

Section 2 demonstrates the key idea by means of a simple example and the concept is generalized in Section 3. Implementation details are discussed in Section 4 and numerical results presented in Section 5. Section 6 concludes the paper with some observations and avenues of future work.

2 Demonstration of the concept by means of an example

Fig. 1 shows a CMOS dynamic logical AND circuit susceptible to charge-sharing noise, and associated waveforms. The first-arriving active-low reset pulse on input R pre-charges the node *N1*, which in turn switches the output node *N2* to a low state. Assume that node *N3* is in a low state due to previous switching history. The subsequently incident active-high pulse on input A switches transistor *Q1* on. Since input B remains low, the nodes *N1* and *N2* are not supposed to switch logical state and the circuit should maintain its reset state.

However, since transistor *Q1* is on, charge-sharing occurs between nodes *N1* and *N3* until both nodes reach an equilibrium voltage. The equilibrium voltage, between the initially high state of node *N1* and the initially low state of node *N3*, is determined by the relative capacitances associated with these nodes. The resulting dip in voltage at node *N1* due to charge-sharing noise is schematically indicated in its waveform. Since node *N2* is low, the small stand-by transistor QS is on. It counteracts the voltage dip on node *N1* and eventually restores both nodes *N1* and node *N3* to the high state. Thus it is imperative that the relative sizing of transistors prevents the dip from causing the output inverter INV to switch. To ensure that the inverter output is stable, the magnitude of the noise dip in the waveform on node *N1* needs to be within the allowed noise margin of the inverter. This noise margin level is indicated as NM_H in Fig. 1.

Assume that the optimization problem for this circuit is as follows:

$$\begin{array}{ll} \min\limits_{x} & t_0(x) \\ \text{s.t.} & v_{N1}(x,t) \geq NM_H \;\forall t \in [t_1, t_2] \end{array} \tag{1}$$

where $t_0(x)$ is the 50% crossing point of the falling voltage transition on node $N2$ and v_{N1} is the voltage on node $N1$, which is a function of the optimization variables $x_i, i = 1, 2, \ldots, 6$ and time t. Assume that the variables of optimization are the widths of the six transistors in the figure (two being inside the inverter).

Problem (1) describes a semi-infinite problem [2, 3], with time as the semi-infinite parameter. The constraint in problem (1) must be satisfied at an infinite number of time points between t_1 and t_2. We reformulate problem (1) as

$$\begin{array}{ll} \min\limits_{x} & t_0(x) \\ \text{s.t.} & c(x) = \displaystyle\int_{t_1}^{t_2} \max\{NM_H - v_{N1}(x,t), 0\} dt = 0 \end{array} \tag{2}$$

wherein the semi-infinite noise constraint of problem (1) has been transformed into an equality constraint involving the time integral $c(x)$. Note that the equality constraint is satisfied if and only if the semi-infinite constraint in problem (1) is satisfied[1]. The

[1]The waveform $v(x,t)$ is a continuously differentiable function of x and t.

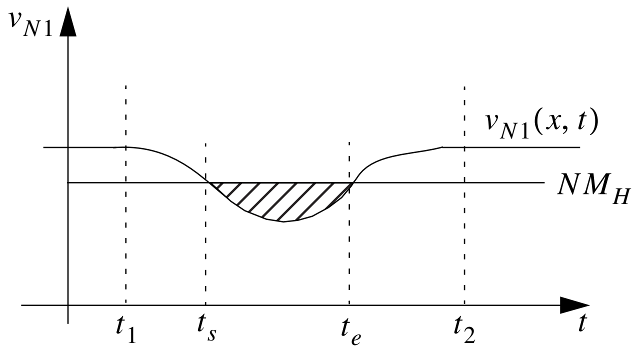

Figure 2: Noise spike in a signal that should be stable.

equality constraint relates to penalty functions for the semi-infinite constraint (see, for example, [7]).

Fig. 2 shows the waveform $v_{N1}(x,t)$, and $c(x)$ is indicated by the shaded area. The constraint in problem (1) is satisfied when this shaded area vanishes. Note that if we run a time-domain simulation of this circuit, $v_{N1}(x,t)$ is known for all time. Time, which is our semi-infinite parameter, is discretized during the simulation, thus making it easy to compute $c(x)$.

Referring to Fig. 2, we can write

$$\begin{aligned} c(x) &= \int_{t_1}^{t_2} \max\{NM_H - v_{N1}(x,t), 0\}dt \\ &= \int_{t_s}^{t_e} \{NM_H - v_{N1}(x,t)\}dt, \end{aligned} \tag{3}$$

where t_s and t_e are the start and end times of the unwanted signal deviation beyond the noise margin. Of course, it is possible that the signal crosses the noise margin multiple times, leading to multiple "noise bumps." In such a case, $c(x)$ is computed as a summation of integrals. For purposes of illustration, this example assumes that there is a single noise bump. Thus, integrating the quantity $\{NM_H - v_{N1}(x,t)\}$ between t_s and t_e yields the required result.

In order to solve problem (2), we also need to provide the gradients of $c(x)$ to the optimizer. We note that $c(x)$ of equation (3) is differentiable. Thus we can write

$$\frac{\partial c(x)}{\partial x} = \frac{\partial}{\partial x}\left[\int_{t_s}^{t_e} \{NM_H - v_{N1}(x,t)\}dt\right]. \tag{4}$$

Note that t_e and t_s themselves are functions of the tunable parameters of the circuit, and hence will change from iteration to iteration of the optimization. Therefore, we cannot differentiate the integral on the right hand side of equation (4) directly. So we rewrite equation (4) as

$$\begin{aligned} \frac{\partial c(x)}{\partial x} = \frac{\partial}{\partial x}\Bigg[\int_{-\infty}^{\infty} &\{NM_H - v_{N1}(x,t)\}* \\ &\{u(t-t_s) - u(t-t_e)\}dt\Bigg], \end{aligned} \tag{5}$$

where $u(t)$ is the unit step function. Then

$$\begin{aligned} \frac{\partial c(x)}{\partial x} &= \left[\int_{-\infty}^{\infty} -\frac{\partial v_{N1}(x,t)}{\partial x}\{u(t-t_s) - u(t-t_e)\}dt\right] \\ &+ \Bigg[\int_{-\infty}^{\infty} \{NM_H - v_{N1}(x,t)\}* \\ &\quad \{-\frac{\partial t_s}{\partial x}\delta(t-t_s) + \frac{\partial t_e}{\partial x}\delta(t-t_e)\}dt\Bigg], \end{aligned} \tag{6}$$

where $\delta(t)$ represents the unit Dirac impulse function. Finally, we obtain

$$\begin{aligned} \frac{\partial c(x)}{\partial x} &= \left[\int_{t_s}^{t_e} -\frac{\partial v_{N1}(x,t)}{\partial x}dt\right] \\ &- \left[\frac{\partial t_s}{\partial x}\{NM_H - v_{N1}(x,t)\}|_{t=t_s}\right] \\ &+ \left[\frac{\partial t_e}{\partial x}\{NM_H - v_{N1}(x,t)\}|_{t=t_e}\right]. \end{aligned} \tag{7}$$

Since the noise deviations at $t = t_e$ and $t = t_s$ are 0 by definition, the final result is

$$\frac{\partial c(x)}{\partial x} = \int_{t_s}^{t_e} -\frac{\partial v_{N1}(x,t)}{\partial x}dt. \tag{8}$$

In the special case when either $t_s = t_1$ or $t_e = t_2$, then the corresponding limit of the integration is not a function of x and the same result is trivially obtained.

We observe that equation (8) requires us to compute the time integral of a voltage gradient, or equivalently the gradient of a time integral of a voltage. The integral form of equation (8) lends itself particularly well to adjoint computations. Transient sensitivities are computed in the adjoint method by expressing each sensitivity function as a convolution integral. A current source of value $-u(t-t_s) + u(t-t_e)$ applied to the measurement node during the adjoint analysis will allow us to obtain the gradients of $c(x)$ with respect to all the variables of the problem in a single appropriately configured [4, 8] adjoint analysis.

Thus we can efficiently compute both $c(x)$ and its gradients. However, in a practical situation, there may be a large number of signals to be checked for noise, and several sub-intervals of time during which the checking must be carried out. Thus the above computations may render the optimization too inefficient to be practical. However, if the optimization algorithm involves repeated minimization of a scalar merit function, we can directly compute the necessary gradients of the merit function rather than those of the individual measurements. For simplicity, suppose we have n noise constrains and the optimizer formulates a Lagrangian merit function

$$\Phi = t_0(x) + \sum_{i=1}^{n} \lambda_i c_i(x), \tag{9}$$

where λ_i are the Lagrange multipliers or dual variables. Then, instead of computing the gradients of $t_0(x)$ and each of the $c_i(x)$, we can compute instead the gradients of Φ by applying the adjoint method of gradient computation [4, 5, 6]. The excitations of the adjoint computation will then be dependent on optimizer variables like the Lagrange multipliers, and will all be *simultaneously* applied. The simulator and optimizer software must cooperate closely in order to apply this method to determine the gradients of Φ. Then, we can compute all the gradients of Φ in a *single* adjoint analysis, irrespective of the number of variables of the problem, irrespective of the number of signals that must be checked for noise, and irrespective of the number of time sub-intervals during which the checking must be carried out!

The following section will expand this key idea to a general circuit optimization problem, with general equality and inequality constraints and possibly objective functions involving noise considerations.

3 Mathematical formulation

Consider a circuit optimization problem

$$\begin{array}{lll}
\min\limits_{x} & \max\limits_{\forall t \in [t_{1_0}, t_{2_0}]} & \max\{v_0(x,t) - k_{2_0}, 0\} \\
\text{s.t.} & c_{e_i}(x) = 0, & i = 1,2,\ldots,E \\
\text{s.t.} & c_{l_i}(x) \leq 0, & i = 1,2,\ldots,L \\
\text{s.t.} & c_{g_i}(x) \geq 0, & i = 1,2,\ldots,G \\
\text{s.t.} & k_{1_n} v_n(x,t) \leq k_{2_n} & \forall t \in [t_{1_n}, t_{2_n}], \\
 & & n = 1,2,\ldots,N.
\end{array} \tag{10}$$

The variables of the problem are denoted by x, $\{v_0(x,t) - k_{2_0}\}$ is a noise function whose positive deviation from zero we wish to minimize, c_e, c_l and c_g are E, L and G equality, less-than and greater-than constraints, respectively, expressed in terms of the circuit measurements. Unlike the simple example of Section 2 which had a single noise constraint, problem (10) has a noise objective function and any number of noise constraints. Each of N noise constraints has four constants associated with it, k_{1_n}, k_{2_n}, t_{1_n} and t_{2_n}. For a signal that should be at a stable logical low, typically $k_{1_n} = 1$ and $k_{2_n} = NM_L$. For a signal that should be at a stable logical high, typically $k_{1_n} = -1$ and $k_{2_n} = -NM_H$.

Problem (10) above is remapped to

$$\begin{array}{ll}
\min\limits_{x,z} & z \\
\text{s.t.} & z \geq \max\{v_0(x,t) - k_{2_0}, 0\} \ \forall t \in [t_{1_0}, t_{2_0}] \\
\text{s.t.} & c_{e_i}(x) = 0, \ i = 1,2,\ldots,E \\
\text{s.t.} & c_{l_i}(x) \leq 0, \ i = 1,2,\ldots,L \\
\text{s.t.} & c_{g_i}(x) \geq 0, \ i = 1,2,\ldots,G \\
\text{s.t.} & k_{1_n} v_n(x,t) \leq k_{2_n} \ \forall t \in [t_{1_n}, t_{2_n}], \\
 & n = 1,2,\ldots,N.
\end{array} \tag{11}$$

This problem is in turn reformulated as

$$\begin{array}{ll}
\min\limits_{x,z} & z \\
\text{s.t.} & z \geq 0 \\
\text{s.t.} & c_0(x,z) = \\
 & \displaystyle\int_{t_{1_0}}^{t_{2_0}} \min[z - \max\{v_0(x,t) - k_{2_0}, 0\}, 0] dt = 0 \\
\text{s.t.} & c_{e_i}(x) = 0, \ i = 1,2,\ldots,E \\
\text{s.t.} & c_{l_i}(x) \leq 0, \ i = 1,2,\ldots,L \\
\text{s.t.} & c_{g_i}(x) \geq 0, \ i = 1,2,\ldots,G \\
\text{s.t.} & c_n(x) = \\
 & \displaystyle\int_{t_{1_n}}^{t_{2_n}} \max\{k_{1_n} v_n(x,t) - k_{2_n}, 0\} dt = 0, \\
 & n = 1,2,\ldots,N
\end{array} \tag{12}$$

and the problem is posed to the nonlinear optimizer as one involving ordinary constraints. The introduced variable z requires initialization, typically at a value that approximates the maximum of $\{v_0(x,t) - k_{2_0}, 0\}$ for the initial value x over the interval $[t_{1_0}, t_{2_0}]$. At each iteration of the optimization, the circuit being optimized is simulated in the time-domain to determine all the measurements of the system. Further, the waveforms $v_n(x,t), n = 0,1,\ldots,N$ are computed for the intervals of time $t_{1_n} \leq t \leq t_{2_n}$. In each such interval, the corresponding waveform is checked to determine the sub-intervals $t_{s_{n_j}} \leq t \leq t_{e_{n_j}}, j = 0,1,\ldots,J_n$ during which $z \leq \max\{v_0(x,t) - k_{2_0}, 0\}$ for $n = 0$[2], or

[2] Our algorithm insists that simple bounds are satisfied, so $z \geq 0$. If not, the definition of $c_0(x,z)$ has to be slightly modified.

$(k_{1_n} v_n(x,t) - k_{2_n}) \geq 0$ otherwise. If the noise objective function or any of the noise constraints involves no such sub-intervals, then the corresponding c_n and its gradients are identically zero. If not, c_n for this iteration of the optimization may be written as

$$c_0(x,z) = \sum_{j=1}^{J_0} \int_{t_{s_{0_j}}}^{t_{e_{0_j}}} \{z - v_0(x,t) + k_{2_0}\} dt, \qquad (13)$$

or

$$c_n(x) = \sum_{j=1}^{J_n} \int_{t_{s_{n_j}}}^{t_{e_{n_j}}} \{k_{1_n} v_n(x,t) - k_{2_n}\} dt, \; n = 1, 2, \ldots, N \qquad (14)$$

and thus easily computed since time is discretized during the time-domain simulation and the voltage waveforms are known. At this point, the original noise objective function has been mapped into a differentiable equality constraint and an objective function comprising of a newly introduced variable and each constraint has been mapped into a differentiable equality constraint.

The next step is to compute the gradients of the merit function of the optimizer. One way to do so is to compute the gradient of each of the objective functions and constraints. The gradients of the regular constraints (c_e, c_l and c_g) are computed by any applicable means. The gradients of the noise constraints of the reformulated problem, c_n, are written (defining $k_{1_0} = -1$) as

$$\frac{\partial c_n}{\partial x} = k_{1_n} \sum_{j=1}^{J_n} \int_{t_{s_{n_j}}}^{t_{e_{n_j}}} \frac{\partial v_n(x,t)}{\partial x} dt, \quad n = 0, 1, \ldots, N \text{ and for all } x, \qquad (15)$$

with $\frac{\partial c_0}{\partial z} = \sum_{j=1}^{J_0} (t_{e_{0_j}} - t_{s_{0_j}})$. Although $t_{s_{n_j}}$, $t_{e_{n_j}}$, z and J_n are functions of x and change from iteration to iteration, Equation (15) above is valid since for each sub-interval, in the case when $n = 0$

$$\text{either } v_0(x, t_{s_{0_j}}) - k_{2_0} - z = 0 \text{ or } t_{s_{0_j}} = t_{1_0} \qquad (16)$$

and

$$\text{either } v_0(x, t_{e_{0_j}}) - k_{2_0} - z = 0 \text{ or } t_{e_{0_j}} = t_{2_0} \qquad (17)$$

or otherwise

$$\text{either } k_{1_n} v_n(x, t_{s_{n_j}}) - k_{2_n} = 0 \text{ or } t_{s_{n_j}} = t_{1_n} \qquad (18)$$

and

$$\text{either } k_{1_n} v_n(x, t_{e_{n_j}}) - k_{2_n} = 0 \text{ or } t_{e_{n_j}} = t_{2_n}. \qquad (19)$$

Note that t_{1_n} and t_{2_n}, $n = 0, 1, \ldots, N$, are not functions of x.

Since the right hand side of Equation (15) is a time integral of a voltage gradient, it is amenable to efficient computation by the adjoint method. The procedure involves attaching a zero-valued current source at each node that has a noise constraint during the nominal transient analysis. During the adjoint analysis, an appropriately scaled pulse of current is applied through this current source in the sub-intervals of time $t_{s_{n_j}} \leq t \leq t_{e_{n_j}}, j = 0, 1, \ldots, J_n$.

As mentioned in the previous section, the gradients of the merit function of the optimizer can be computed by means of a single adjoint analysis. In this situation, the $c_n(x)$ constraints are treated as ordinary equality constraints. At each iteration, $c_n(x)$ is expressed as a summation of time integrals (Equations (13) and (14)) and a single adjoint analysis is applied to obtain the gradients of the merit function of the optimizer by appropriate choices of adjoint excitations [4, 5, 6].

In the case where the optimization merit function does not involve any semi-infinite component it can be dealt with directly [5, 6]. In addition, we note that the following three types of objective functions are readily accommodated by appropriate introductions of auxiliary variables and constraint definitions.

$$\min_x \max_t \; |v_0(x,t) - k_{2_0}| \qquad (20)$$

$$\min_x \max_t \; v_0(x,t) \qquad (21)$$

$$\max_x \min_t \; \min\{v_0(x,t) - k_{2_0}, 0\} \qquad (22)$$

$$\max_x \min_t \; v_0(x,t) \qquad (23)$$

Thus the method of incorporating noise constraints applies to any number of noise constraints and objective functions and any number of unwanted signal deviations during the time period of each noise consideration. Further, the computation of gradients by means of a single adjoint analysis can be applied irrespective of the number of measurements, the number of ordinary constraints, the number of noise constraints and the number of objective functions. Further, the concept can be applied to any differentiable merit function such as penalty or barrier merit functions (referred to as interior and exterior techniques in [9]).

4 Implementation

The method proposed in this paper was implemented in the JiffyTune framework [10, 5, 6]. This section presents a short description of JiffyTune and then mentions some salient points of the implementation of noise-aware circuit optimization. JiffyTune optimizes circuits by adjusting transistor and wire sizes. Delay, slew, power, area and noise considerations are presently supported. JiffyTune allows flexible definition of objective functions and constraints. Further, minimax optimization is supported and is typically used to minimize the worst of several path delays. The minimax capability can now also be used to minimize the worst of several noise violations. JiffyTune uses the general-purpose nonlinear optimization package LANCELOT [11, 12, 13] and fast simulation [14] and adjoint gradient computation [8, 15] in SPECS. The adjoint Lagrangian method of gradient computation [5, 6] is used to efficiently determine the gradients of the merit function of LANCELOT. Several special considerations to render the optimization efficient [16], tailor the optimization to the circuit tuning task [6], stop the optimization at a meaningful point [10] and customize Hessian updates [5, 6] to the adjoint Lagrangian computations have been implemented in JiffyTune.

JiffyTune includes a graphical user-interface in the Cadence schematic environment. The interface allows convenient specification of circuit optimization problems and visualization of tuning results. "Grouping" of similar structures and ratio-ing of individual transistors are allowed.

JiffyTune has successfully been used to tune high-performance circuits of PowerPC and S/390 microprocessors. Circuits with over 10,000 tunable transistors have been tuned in a few hours of CPU time. JiffyTune has also been helpful in understanding the tradeoffs inherent in circuit designs. It has proved useful for circuit re-use in the case of changed requirements, changed loading conditions or remapping to a new technology. All the tuning criteria are stored as attributes of the schematic in order to facilitate design re-use.

As indicated above, noise considerations are implemented by first converting them to time-integral constrains. Zero-valued current sources are added at the noise measurement points. The integrals are evaluated on the fly during the nominal simulation in SPECS at each iteration of LANCELOT. Further, the crossing times ($t_{s_{n_j}}$ and $t_{e_{n_j}}$ of the previous section) are stored during the nominal simulation. Before the adjoint simulation begins, the excitations to be applied on the auxiliary current sources are determined. These excitations are typically scaled and shifted unit-step functions, with the durations determined by the crossing times.

Then the adjoint analysis is carried out with these additional excitations representing the contributions of the noise functions to the overall merit function. Convolution between the nominal and adjoint waveforms is carried out for each parameter to determine the required time-domain sensitivities. Extensive chain-ruling is employed to determine the gradient of the merit function with respect to all the ramifications of changing a parameter. For example, changing a transistor width changes the channel current, the intrinsic MOS parasitic capacitances and the associated diffusion capacitances. All these effects are combined to obtain the final gradient vector used by LANCELOT to compute the next step of the optimization.

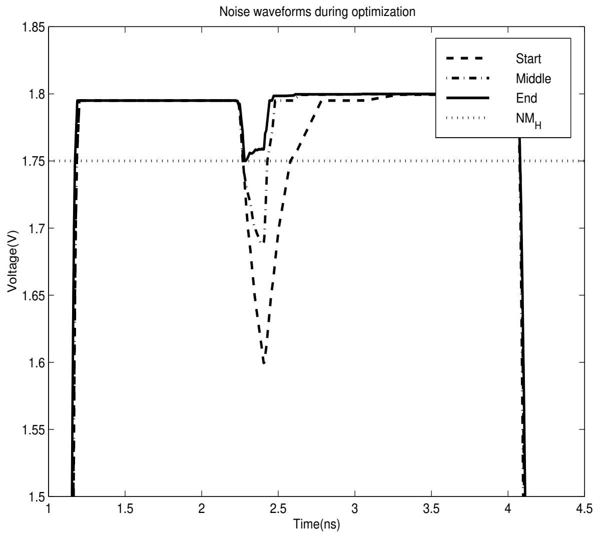

Figure 3: Reduction of noise during iterations of the optimization.

5 Results

The circuit in Fig. 1 was optimized to minimize the worst-case delay from the data inputs to the output, while constraining the area (as modeled by the sum of the tunable transistor widths) and ensuring that the intermediate node *N1* conformed to tight noise constraints. JiffyTune solved the problem in 9 iterations. Snapshots of the waveform on node *N1* at the start, middle and end of the optimization are shown in Fig. 3. The horizontal line in the figure shows the noise margin NM_H specified. As the optimizer progresses, devices are sized to make the noise violation smaller, until eventually the voltage is entirely above NM_H during the specified time period.

In a separate set of experiments, JiffyTune was used to study the delay vs. noise tradeoff in a dynamic AND gate. The circuit of Fig. 1 was tuned in a realistic circuit environment to minimize the switching delay from the data input A to the output, with a noise constraint on node *N1* and a 200 ps constraint on the delay from the reset signal falling to the output node falling. The P to N ratio of the output inverter was constrained to

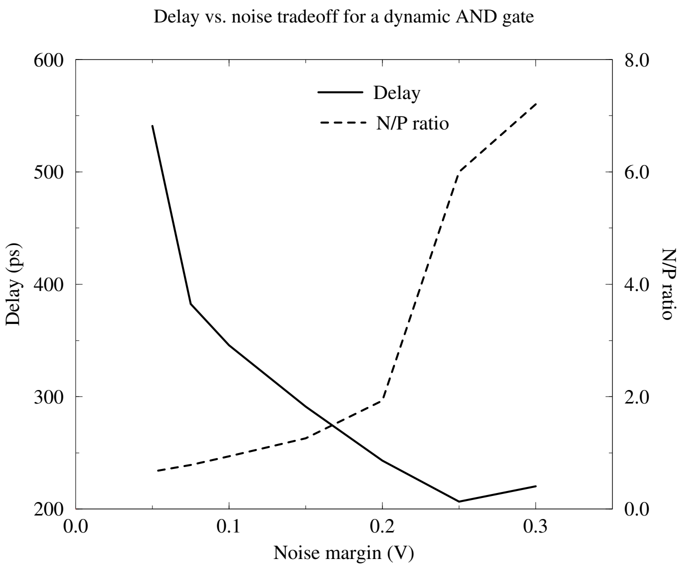

Figure 4: Delay vs. noise tradeoff for a dynamic AND gate.

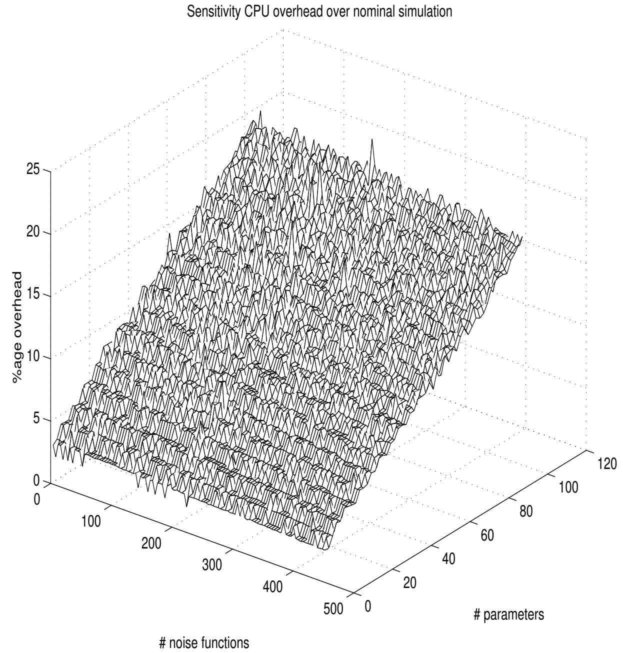

Figure 5: Growth of CPU time with the number of parameters and noise functions.

be no larger than 4 to maintain balance between the rise and fall times of *N2*. The required noise margin ($V_{dd} - NM_H$) on *N1* was varied from 50 mV to 300 mV and a series of circuit optimization runs were performed. Fig. 4 shows the results of this experiment. The solid line shows the variation of delay (including one inverter stage through which the input signals are fed) with noise margin and the ratio of the width of *Q1* to that of the stand-by transistor *QS* is shown with a dotted line. As the noise margin is loosened, the optimal delay of the gate improves and the N/P ratio gets larger since *QS* can be made smaller to meet a less stringent noise criterion. At a noise margin of about 250 mV, the best possible delay is obtained, and the ideal N/P ratio is in the neighborhood of 5.5. Beyond that, the PFET *QS* is at its minimum width and no further improvement in delay is possible, since noise is no longer the limiting factor. In this manner, JiffyTune can be used to study tradeoffs between delay and noise (and of course, area and power) during library design of dynamic cells.

To test the efficiency of incorporating a large number of noise constraints, the following experiment was carried out. A dynamic logic "branch-scan" circuit with 144 MOSFETs was configured with 36 delay measurements, each of which is treated as a sensitivity function. The number of tunable transistors was varied from 1 to 104, and the number of noise functions on various signals during various sub-intervals of the simulation was varied from 1 to 459. For each such combination, simulation and gradient computation were carried out. The gradient computation was in "adjoint Lagrangian" mode whereby the gradients of LANCELOT's merit function were computed in a single adjoint analysis. In each run, the overhead of the run time for gradient computation over the run time for nominal transient simulation was determined. Fig. 5 plots the overhead as a percentage, as a function of the number of noise functions (over and above the 36 delay functions) and the number of tunable transistors. As can be seen from the figure, the overhead changes from 3% to 18% as the number of parameters is increased from 1 to 104. For each new parameter, an additional convolution must be carried out between the waveforms of the nominal and adjoint circuits. The larger number of convolutions accounts for the increase in overhead with the number of parameters. However, even with 104 parameters, the overhead is a modest 18% over the nominal transient simulation. More importantly, the increase in CPU time with additional noise functions is negligible since a single adjoint analysis is conducted irrespective of the number of such functions! Thus a large number of noise considerations can be incorporated with a very small impact on run time. (The noisy nature of the data in Fig. 5 is due to the granularity of CPU time measurements.)

6 Conclusions and future work

Noise considerations are an increasingly important part of modern integrated circuit design. Ideally, automatic optimization of circuits should take into account noise objective functions and noise constraints. Since noise considerations give rise to semi-infinite problems, they are hard to incorporate during circuit optimization. In this paper, we presented a method to remap these noise considerations to time-integral equality constraints. The problem then becomes amenable to solution by a standard nonlinear optimizer, provided we can compute gradients. By using the adjoint method to directly compute the gradients of the optimizer's scalar merit function, we showed that all the required gradients can be computed during a single adjoint analysis of the underlying circuit, thus rendering the process feasible and practical. The method is applicable to different types of noise, general circuitry and a general choice of merit function.

The method of incorporating noise considerations presented in this paper can be applied to any type of circuit optimization that uses simulation in the inner loop, including optimization based on static timing analysis [17]. Timing analysis and tuning of custom high-performance circuitry is often performed by simulating "channel-connected components" in the time-domain. The methods in this paper can be applied to optimally size large circuits to avoid noise problems, to understand tradeoffs in the design of library cells, to optimally space wires to avoid coupling noise and in package design. Noise measures such as the "noise stability" criterion of [1] can be appropriately translated into semi-infinite constraints and are then amenable to the methods described in this paper. Electromigration constraints that limit peak current density can be incorporated by the methods described in this paper, too.

The generation of the list of noise constraints for a large circuit can be a tedious job. Automation of the specification of noise considerations during circuit optimization would make the noise-aware optimization capability easier to use and conducive to productive design.

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References

[1] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design," *IEEE International Conference on Computer-Aided Design*, pp. 524–531, November 1996.

[2] R. Hettich, *Semi-infinite programming.* No. 15 in Lecture notes in Control and Information Sciences, Springer Verlag, 1979.

[3] R. Hettich and K. O. Kortanek, "Semi-infinite programming: theory, methods, and applications," *SIAM Review*, vol. 35, pp. 380–429, September 1993.

[4] S. W. Director and R. A. Rohrer, "The generalized adjoint network and network sensitivities," *IEEE Transactions on Circuit Theory*, vol. CT-16, pp. 318–323, August 1969.

[5] A. R. Conn, R. A. Haring, C. Visweswariah, and C. W. Wu, "Circuit optimization via adjoint Lagrangians," *IEEE International Conference on Computer-Aided Design*, pp. 281–288, November 1997.

[6] A. R. Conn, P. K. Coulman, R. A. Haring, G. L. Morrill, C. Visweswariah, and C. W. Wu, "Jiffytune: circuit optimization using time-domain sensitivities," *IEEE Transactions on Computer-Aided Design of ICs and Systems*, 1998. To appear.

[7] A. R. Conn and N. I. M. Gould, "An exact penalty function for semi-infinite programming," *Mathematical Programming*, vol. 37, no. 1, pp. 19–40, 1987.

[8] P. Feldmann, T. V. Nguyen, S. W. Director, and R. A. Rohrer, "Sensitivity computation in piecewise approximate circuit simulation," *IEEE Transactions on Computer-Aided Design of ICs and Systems*, vol. 10, pp. 171–183, February 1991.

[9] A. V. Fiacco and G. P. McCormick, *Nonlinear programming: sequential unconstrained minimization techniques.* New York: John Wiley and Sons, 1968. Reprinted as *Classics in applied mathematics 4*, SIAM, 1990.

[10] A. R. Conn, P. K. Coulman, R. A. Haring, G. L. Morrill, and C. Visweswariah, "Optimization of custom MOS circuits by transistor sizing," *IEEE International Conference on Computer-Aided Design*, pp. 174–180, November 1996.

[11] A. R. Conn, N. I. M. Gould, and Ph. L. Toint, "Global convergence of a class of trust region algorithms for optimization with simple bounds," *SIAM Journal on Numerical Analysis*, vol. 25, pp. 433–460, 1988. See also same journal, pp. 764–767, volume 26, 1989.

[12] A. R. Conn, N. I. M. Gould, and Ph. L. Toint, "A globally convergent augmented Lagrangian algorithm for optimization with general constraints and simple bounds," *SIAM Journal on Numerical Analysis*, vol. 28, no. 2, pp. 545–572, 1991.

[13] A. R. Conn, N. I. M. Gould, and Ph. L. Toint, *LANCELOT: A Fortran Package for Large-Scale Nonlinear Optimization (Release A).* Springer Verlag, 1992.

[14] C. Visweswariah and R. A. Rohrer, "Piecewise approximate circuit simulation," *IEEE Transactions on Computer-Aided Design of ICs and Systems*, vol. 10, pp. 861–870, July 1991.

[15] T. V. Nguyen, "Transient sensitivity computation and applications," Tech. Rep. CMUCAD-91-40, Carnegie Mellon University, Pittsburgh, PA, 1991.

[16] A. R. Conn, L. N. Vicente, and C. Visweswariah, "Two-step algorithms for nonlinear optimization with structured applications," *SIAM Journal on Optimization*, 1998. Submitted for publication, under review.

[17] C. Visweswariah, "Optimization techniques for high-performance digital circuits," *IEEE International Conference on Computer-Aided Design*, pp. 198–205, November 1997.