Retiming Review

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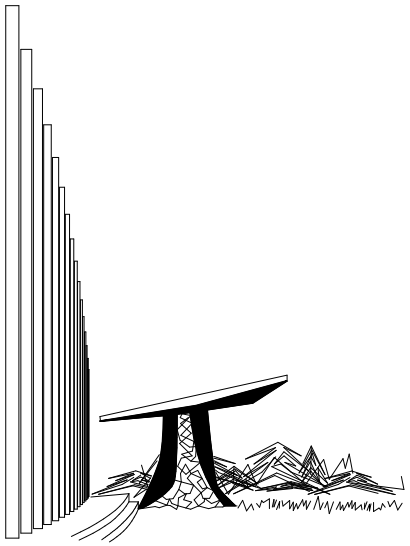

OUTLINE

- Retiming is a powerful optimization
  - –> Gets optimization in sequential domain
- Solid Mathematical Foundation
  - –> Many polynomial optimizations
- Still not widely applied
  - –> Practical Problems

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RETIMING IS POWERFUL

- Area
- Timing
- Power
- Test

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SOLID MATHEMATICAL FOUNDATION

- Min Delay [Leis83, Leis91]
- Min. registers under delay constraint [Leis]
- Efficiency [vdWerf94], [Shenoy94]
- Clock Skew equivalence [Martin93]

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PRACTICAL PROBLEMS

- Initial States [Touati93] [Stok95] [Singhal95]
- Fanout Problem [Lalgudi95]
- Tricky Clocking Schemes [Lockyear92, Ishii92, Papae93]
- Verification [Shenoy92] [Kostelijk93]
- Joint objective optimization
- Interaction with combinatorial optimization
  [Malik93], [Weinman93], [Grodstein94]
- Clock Gating Problems [Ploger92]
- Logic included in latches
- .....

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INITIAL STATES

- Initial States not well defined [Singhal95]

  => delayed equivalence

- Initial States are Important [Stok95, Even96]

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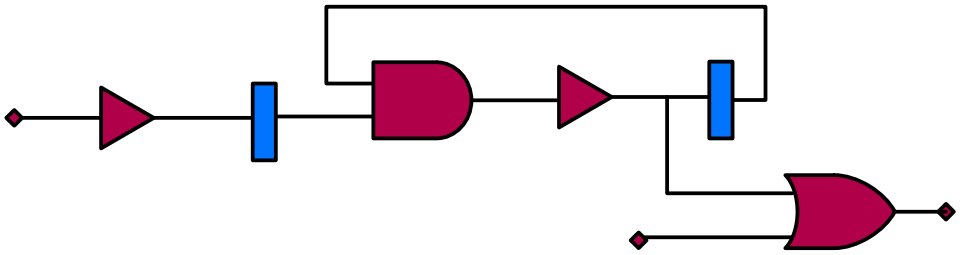
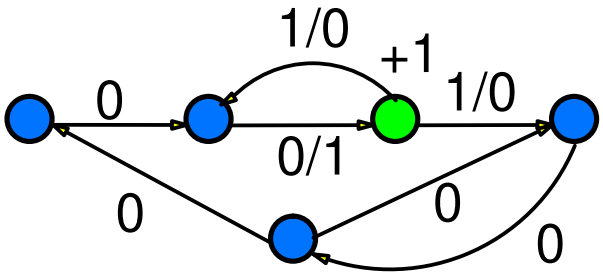
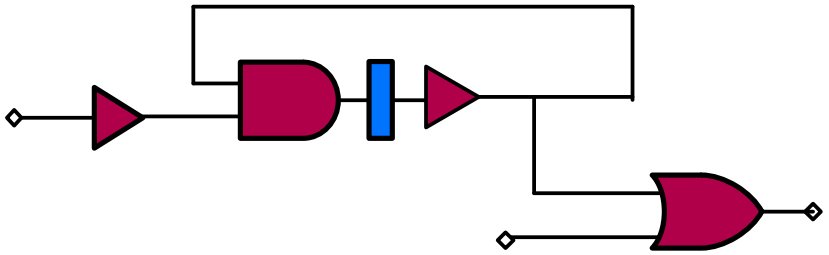
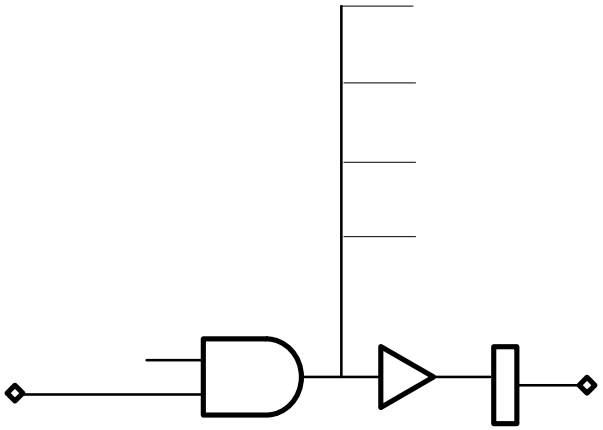
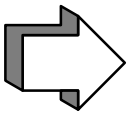
FANOUT PROBLEM

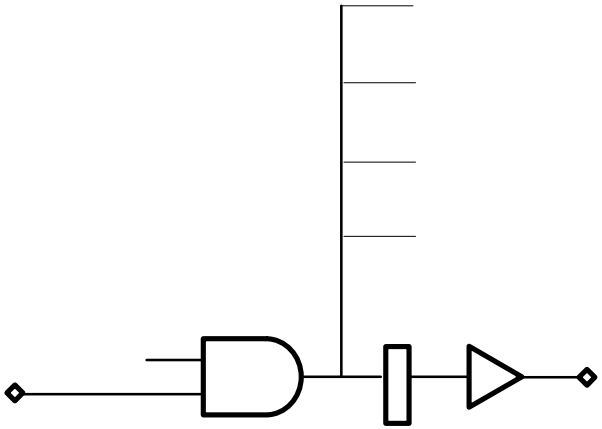












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CLOCKING SCHEMES

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VERIFICATION

- Isomorphism testing and testing of # latches in loops (io−paths) is not sufficient.
- General (combinational) verification strategy required.

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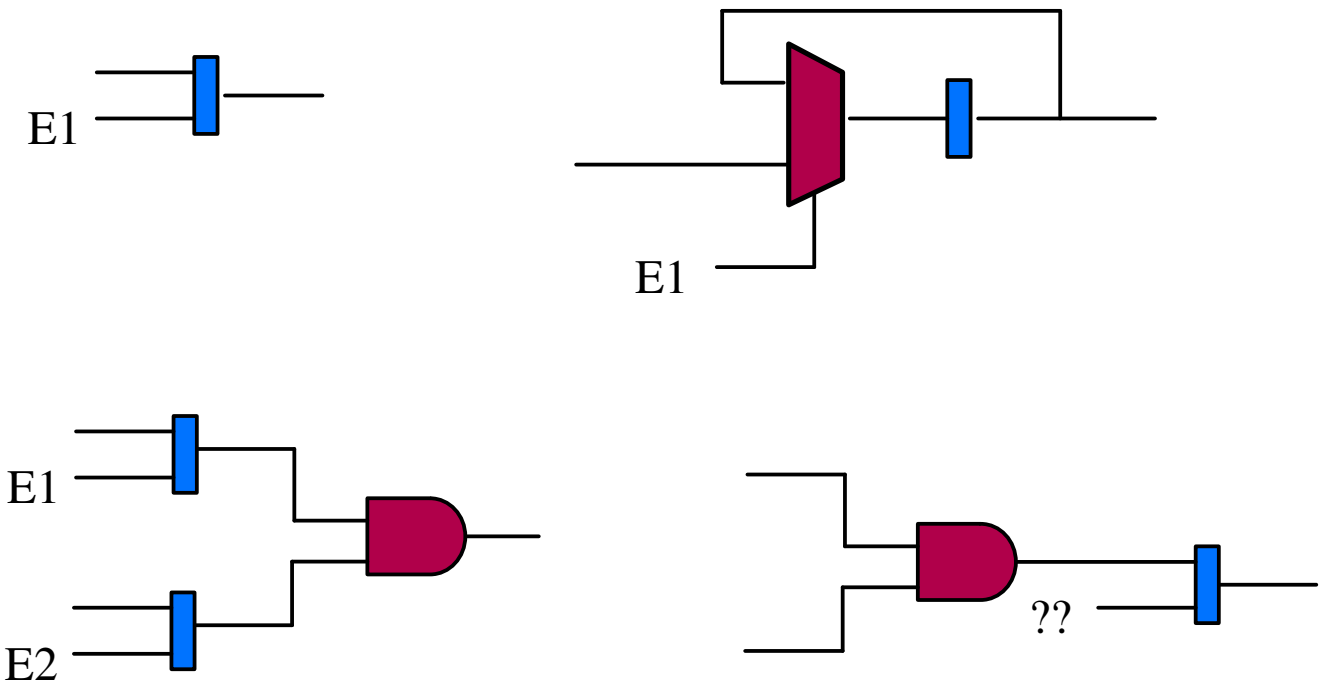
CLOCK GATING



Props:
– can only retime if registers have equal enable signals
– can not retime past its enable signal.

– Easy to test local
– How to incorporate into global algorithm ?

[Ploger92]

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INTERACTION WITH COMBINATORIAL OPTIMIZATION

- When and where in synthesis flow ??
- Peripheral retiming [Malik93]
- Retiming and Tree Mapping [Grodstein94]
- FPGAs [Weinman93]

LOGIC INCLUDED IN LATCHES

- Simple logic functions: and/or/nand
- Complex logic functions, muxes
- Extreme FPGA's

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CONCLUSIONS

- Retiming is a powerful transformation to extend practical optimization into the sequential domain
- Mathematical Foundations have been laid
- Several of the practical problems have been addressed
- Many more need to follow to enable widespread use in logic synthesis systems.

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