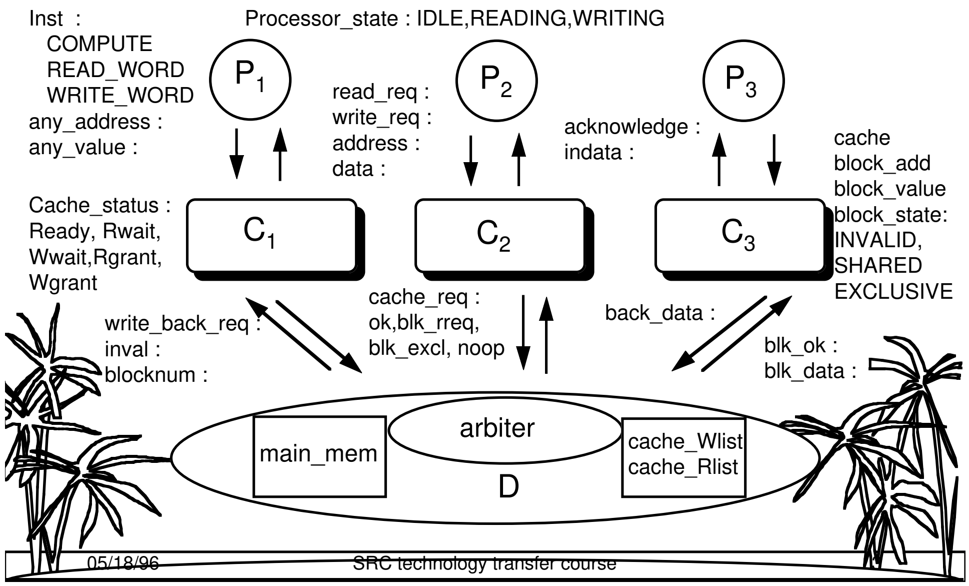
Example: Cache Coherance in a Multiprocessor System

Gitanjali M. Swamy
The VIS Group
Dept of Electrical Engg and Computer Sciences

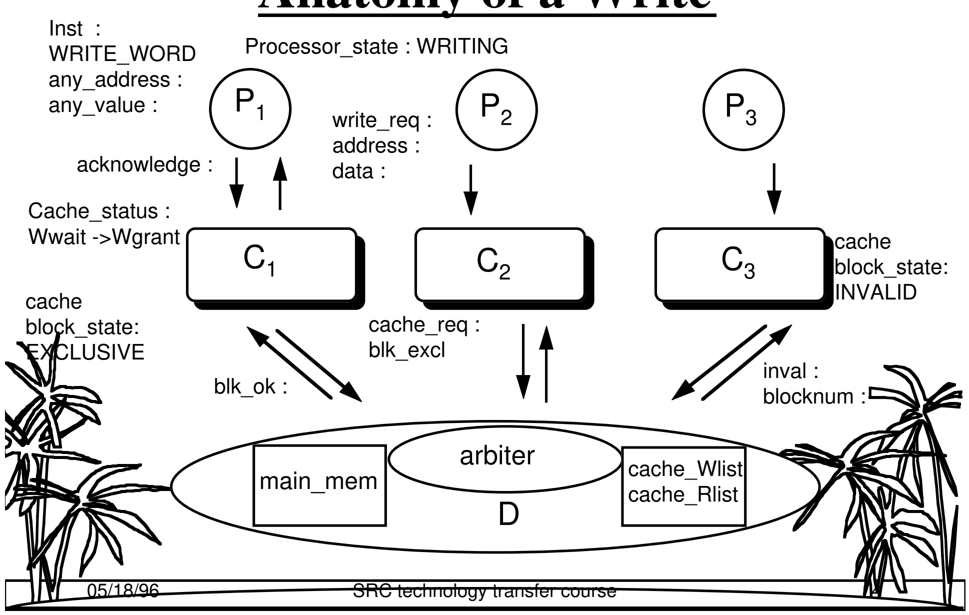
Model: Multiprocessor System

- Components:
  - Processors P_i
  - Caches C_i
  - Directory + Arbiter +Main Memory D
- Cache Coherancy Problem: Processors are writing and reading from same memory. Need to ensure that correct data is read by each processor.

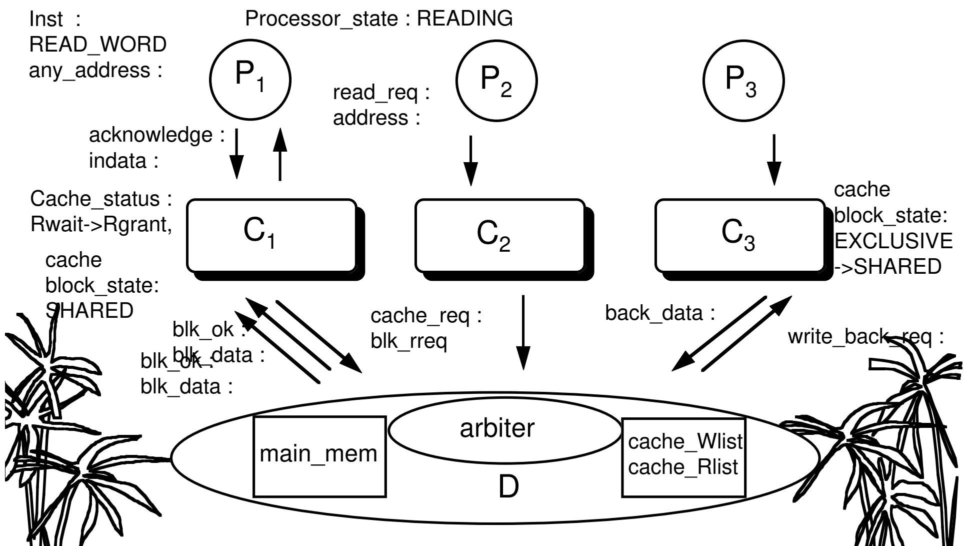
Model: A Multiprocessor System



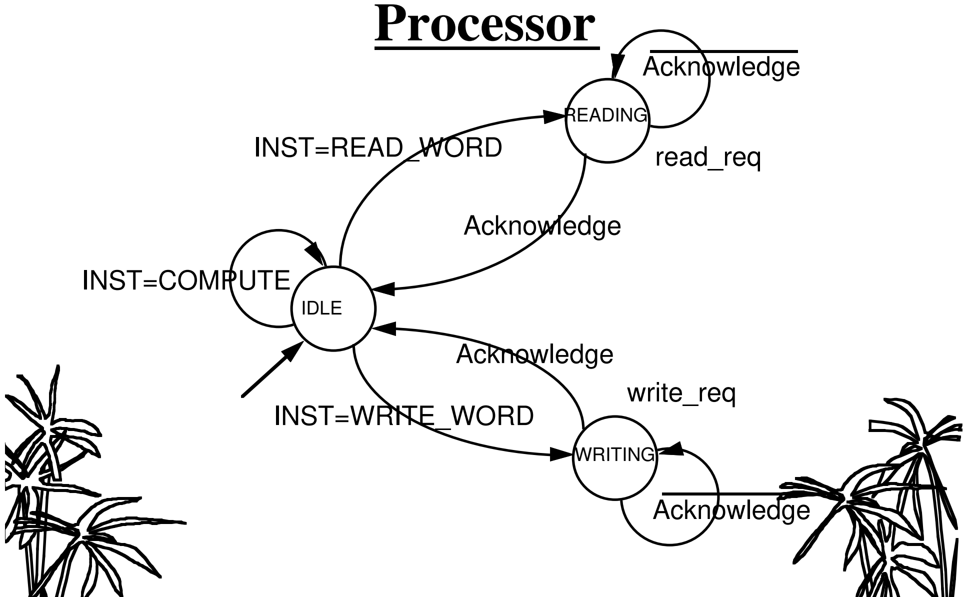
Anatomy of a Write



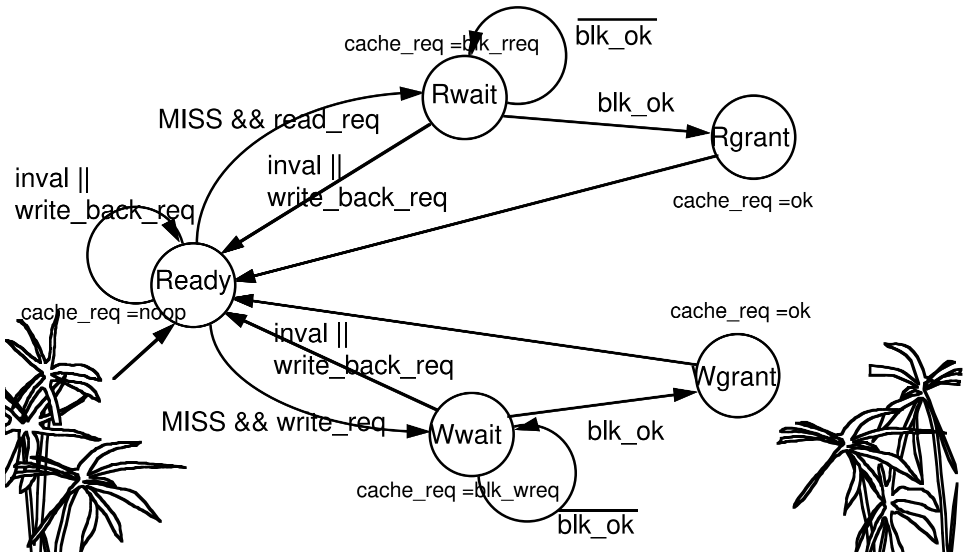
Anatomy of a Read



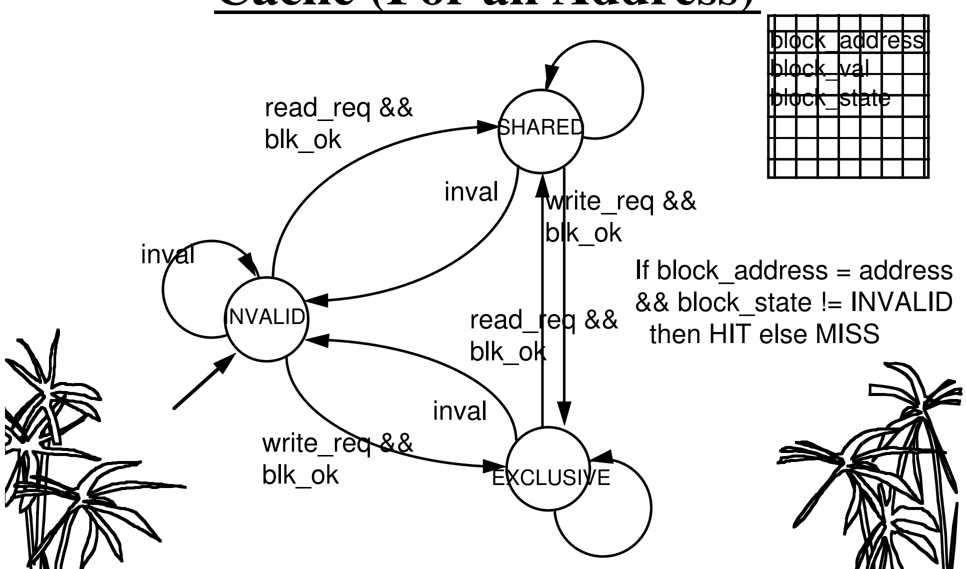
Processor



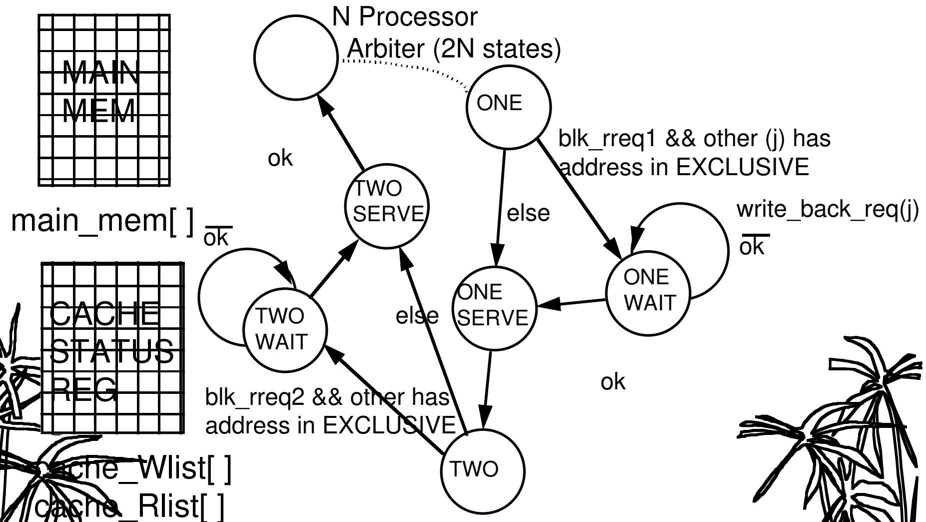
Cache Controller



Cache (For an Address)



Directory+Main Memory +Arbiter



Simplifying Assumptions

- Number of Processors = 2
- Size of Cache = 1
- Size of Main Mem = 2

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Properties

- Some correctness criteria:
  - Two caches cannot be simultaneously in EXCLUSIVE for the address 0.
- AG(((cc1.block_state = EXCLUSIVE) * (cc2.block_state = EXCLUSIVE)) -> ((cc1.block_address =0)*(cc1.block_address=0)))
  - The cache state stored in the directory and the cache actual state must be consistent .

Properties

- A memory system is Coherent if
  - A READ by P_i to X that follows a WRITE by P_i to X (X=A), with no WRITE by other P_k return value A.
  - A READ by P_i to X that follows a WRITE by P_k to X (X=A), returns value A.
  - WRITEs to X by P_i , P_k are serialized.

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Exercise

- Read Verilog code, convince yourself of the correlation with FSM's.
- Read into VIS, and compute reached states (will take too long). Try re-ordering
- Read given ordering and compute reached states.
- Simulate design to attempt to see if properties (english) specified hold.

Exercise(cont)

- Formulate properties in CTL, and model check.
- Does the design satisfy the property ?
- If not modify the design to make property pass.
- Note that arbiter is inefficient. Construct a more efficient arbiter.
- Write a property to show your arbiter is better.

A Few Pointers

- Make sure your CTL formulae refer to the Blifmv variable names (These are not the same as Verilog names).
- Use the ordering file provided.
- Remember that latched variables are output at the next clock cycle, but wires are output immediately.
- Keep in mind your property may be wrongly formulated.