

Platform Design for Swarm Wearable Computing

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ABSTRACT

Wearable computers can provide continuous intelligent real-time monitoring of the human body, enabling a large variety of new applications in several domains including wellness and health care. The key notion of Swarm Wearable Computing is ubiquitous intelligent embedded processing for sensing, monitoring and logging of data about human activity. This paper provides a discussion of the design challenges associated with our vision of “swarm” integrated wearable computers and a holistic approach to programmable ASIC design. An ultra-low power signal processing SoC capable of processing tri-axial accelerometer data for human activity recognition is presented. Technological hurdles like ease-of-use, device lifetime, and form factor as well as critical issues for “swarm” devices are considered. Programmability and adaptability of signal processing, energy aware power management and control, and hardware optimization are crucial to the realization of our vision of a single chip solution. Our core signal processing architecture has been implemented in C and significant progress has been made on a behavioral Verilog description. The ultimate goal of this project is CMOS fabrication of a fully integrated SoC including embedded processing, sub-threshold SRAM, wireless connectivity, energy harvesting, power management, and battery-on-chip.

1. INTRODUCTION

SWARM WEARABLE COMPUTERS have tremendous potential to solve some of society’s most challenging problems, by integrating technology with our biological and physical world. Significant advancement of semi-conductor research has enabled System on Chip (SoC) wireless devices to be embedded with powerful micro-computers and a variety of sensors, in a miniature wearable form factor. These devices can provide continuous intelligent monitoring and logging of bio-signal data for a variety of applications. The key notion of Swarm Wearable Computing “SwarmWear” is ubiquitous embedded processing, sensors, and control. “Swarms” of wearable computers can provide an unprecedented amount of information about human activity and health. The vast quantity of diverse patient data stored “in the cloud”, promises to impart new insights in treatment and prevention of many illnesses [5]. By providing regular feedback, these devices can help individuals be far more aware of their health and adaptive to the needs of their bodies. When fully realized, swarms of wearable computers can be used for a variety of applications.

What differentiates “swarm” applications from other wireless sensor network/node concepts? Swarm applications share resources, such as sensors, computing power, data storage, etc. In the “swarm” world there are “cyber-interfaces” everywhere that provide both human-cyber and cyber-biological/physical interaction. This approach leads to a platform vision “swarmOS” that allows for more efficient use of the available resources, essentially separating the application developer from the complexities of hardware and resource management [5]. Despite the great enthusiasm for the concept of ubiquitous swarm devices among the academic community, there are several issues that have hindered widespread adoption. Ease-of-use, security, lifetime, wear-ability, and form factor are some of the technological issues,

as discussed in similar work [3]. If SwarmWear applications are to succeed, they should be designed for “swarmOS” interaction, while also resolving the technical issues. We envision a holistic approach to the design with these core principles:

- Provides for programmability and flexibility of cyber-physical interactions and can be adapted to the application.
- Supports energy aware control of the system and core signal processing algorithms and uses energy harvesting for potentially indefinite lifetime.
- Integrates efficient hardware and logic design techniques for optimal energy usage, form factor and wear-ability.

2. DESIGN OVERVIEW

Activity recognition using wearable computers can be used for a variety of applications, such as exercise monitoring, quality of life improvement for elderly, early detection of the onset of illnesses and many more. Activity recognition refers to using inertial data to detect specific movements such as “sit to stand”, “stand to lie”, “walking”, etc. [1]. By combining an interesting application with the core design principles, we are developing an ultra-low power wearable computer SoC capable of acquiring and processing three axis accelerometer data using the Dynamic Time Warping algorithm. The ultimate goal is a one-chip-solution, with integration of embedded processing, custom SRAM and/or FRAM, wireless communication, energy harvesting, power management, and battery-on-chip. Similar work has shown that it is possible to integrate essential components and enables ultra-low power battery less signal processing [3].

To maintain the modular nature of this swarm device and to provide the developer options, we have worked to keep the system and control as open as possible. An energy aware controller uses a decision model to optimize between signal processing accuracy and energy usage. By monitoring energy availability and consumption, the controller can efficiently utilize computational resources to improve lifetime. Our hardware design approach uses circuits that are more energy efficient at the cost of delay. In the context of this application, high performance is unnecessary. We present a comprehensive top-down approach, critical to the success of SwarmWear systems, with key focus on adaptability, signal processing algorithms and hardware.

3. APPLICATION AND ADAPTABILITY

Swarm integration of wearable computers demands a highly flexible and open design approach. These devices must be able to provide computational resources on demand, and will likely require wireless re-configurability [5]. In the context of this application, activity recognition requires pre-training of specific movements, which are stored on the device. Training takes time, and not all trained movements work for all people. This forces the need for individual training, which is constrained by how difficult it is for the user. To resolve this, we introduce a concept called cross swarm optimization. Essentially, sharing trained movements between devices provides a much more robust training set, which can easily be updated from the cloud.

As another example of the need for adaptability, we envision multi-modal operation for emergency scenarios. In the event of a

natural disaster wearable computers may be used to monitor the condition of potential victims. Leveraging maximum computational resources would keep emergency responders better informed to allocate emergency resources most effectively. In context of activity monitoring, it would be important that movements which indicate a person is in perilous danger have highest priority, to minimize recognition time. One can imagine a variety of similar challenging applications, which is why designing for platform abstraction is crucial for swarm devices.

4. SIGNAL PROCESSING ALGORITHMS

Activity Recognition is the targeted application for this project, which is accomplished by comparing incoming accelerometer data to pre-trained “template” movements and assigning a score. The algorithm used is called Dynamic Time Warping (DTW). It was developed in the 1980’s for early speech processing, and has gained interest in recent years for processing of highly time dependent signals [4].

An intelligent signal processing architecture should provide tunable parameters that allow flexibility between performance (speed), power consumption, and classification accuracy. These parameters allow algorithms to be reconfigured for the needs of the application. To demonstrate this concept, we use a technique called Granular Decision Making, proposed in [2]. Uninteresting movements are removed as early as possible using low resolution and sampling rate, and only interesting movements are with higher accuracy [2]. This approach uses tunable parameters including resolution, sampling frequency, threshold, and movement priority. Modification of the parameters provides developers with significant flexibility and allows the system to adapt to the energy conditions.

5. ARCHITECTURE

Providing flexibility and programmability can be challenging in a SoC solution. Microcontrollers offer programmability in a much simpler implementation, but typically have higher power consumption. In contrast a fully ASIC chip offers very low power, but is more difficult to design and has limits to the flexibility of the system [1]. We propose a merging of the two to provide some flexibility while also extremely low power. Other work has demonstrated an ultra-low power wireless streaming signal processing SoC, allowing for battery-free operation and promising indefinite lifetime and optimal form factor. [3]. Despite the promising results, the design offers limited adaptability. For SwarmWear applications, algorithms need to be adaptable to a variety of applications, which for an ASIC chip would require a full redesign.

The proposed programmable ASIC hybrid architecture is adaptable to a variety of applications. Signal processing is broken up into functional blocks, enabling modular control and reconfigurable algorithms. Signal processing cores need only contain minimum intelligence while still meeting the needs of the application. Using short instructions containing processing tasks to be executed, the controller can simply request resources, and monitor the results. This is achieved using event based processing. A reconfigurable low quality preprocessing block identifies potential movements. When this occurs an event is spawned. Events are analyzed and prioritized using a decision matrix and then processed with higher quality. Tethering potential movements to an event object encourages highly parallelized and adaptive processing.

6. HARDWARE DESIGN

High performance processing is not required in body monitoring applications due to the infrequent nature of the activities being

monitored [2]. Minimization of the form factor and extending device lifetime are critical concerns, so when designing hardware power optimization is crucial. Low performance requirements enable reduction of the supply voltage for sub-threshold operation, which provides significant power reduction as shown state-of-the-art work [3]. Various design challenges include supply voltage fluctuations and total power loss. To address these challenges, custom hardware should be used. This approach leverages asynchronous circuits, sub-threshold SRAM, and sleep mode. Further discussion of an asynchronous approach is beyond the scope of this discussion and will be including in future papers.

Designing SRAM to operate in sub-threshold region can be challenging as traditional designs have stability issues at low voltages. Energy usage, reliability and robustness are key concerns. We designed an SRAM which features a new 11-transistor memory cell, to eliminate contention during read or write cycles, essentially maximizing the noise margin. New column circuitry utilizes static logic as opposed to the common dynamic logic, as the latter is far more susceptible to failures. The proposed SRAM has been simulated at extremely low voltage, and consumes very low power while running at minimum operating voltage.

7. DISCUSSION AND FUTURE WORK

We have presented core principles of an application that provides an ultra-low power solution for wearable computers that are adaptable to the swarm. SwarmWear challenges were discussed as well as our holistic approach to design of a programmable ASIC wearable computer. To allow for optimally efficient algorithms, our signal processing core provides tunable parameters for dynamic and flexible Granular Decision Making. By providing energy awareness to the control system, it can adjust and reallocate processing resources for optimal energy usage. Our core signal processing architecture has been implemented in C and significant progress has been made on a behavioral Verilog description, with RTL to follow. Our initial design and fabrication will be a proof of concept and sub-threshold SRAM, but future designs will implement asynchronous logic for very low voltage operation. The ultimate goal of this project is fabrication in commercial CMOS technology of a fully integrated SoC including embedded processing, sub-threshold SRAM, wireless connectivity, energy harvesting, power management, and battery-on-chip.

REFERENCES

- [1] Bidmeshki M M, Jafari R. Low Power Programmable Architecture for Periodic Activity Monitoring. In *Proceedings of the ACM/IEEE 4th International Conference on Cyber-Physical Systems (ICCPS '13)*. 2013.
- [2] Ghasemzadeh H, Jafari R. Ultra low power signal processing in wearable monitoring systems: A tiered screening architecture with optimal bit resolution. *ACM Transactions in Embedded Computing Systems (TECS)*.
- [3] Zhang Y, Zhang F, Shakhsher Y, et al. A battery-less 19 W MICS/ISM-band energy harvesting body sensor node soc for EXG applications. *Solid-State Circuits, IEEE Journal of*, 2013, 48(1): 199-213.
- [4] Myers C, Rabiner L, Rosenberg A. Performance tradeoffs in dynamic time warping algorithms for isolated word recognition. *Acoustics, Speech and Signal Processing, IEEE Transactions on*, 1980, 28(6): 623-635.
- [5] Lee E A, Kubiatowicz J D, Rabaey J M, et al. The TerraSwarm Research Center (TSRC) (A White Paper). Technical report UCB/EECS-2012-207, 2012.